A 640 × 512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC

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***Abstract*—Analysis results demonstrate that multiple sampling can achieve consistently higher signal-to-noise ratio at equal or higher dynamic range than using other image sensor dynamic range enhancement schemes such as well capacity adjusting. Implementing multiple sampling, however, requires much higher readout speeds than can be achieved using typical CMOS active pixel sensor (APS). This paper demonstrates, using a 640 × 512 CMOS image sensor with 8-b bit-serial Nyquist rate analog-to-digital converter (ADC) per 4 pixels, that pixel-level ADC enables a highly flexible and efficient implementation of multiple sampling to enhance dynamic range. Since pixel values are available to the ADC's at all times, the number and timing of the samples as well as the number of bits obtained from each sample can be freely selected and read out at fast SRAM speeds. By sampling at exponentially increasing exposure times, pixel values with binary floating-point resolution can be obtained. The 640 × 512 sensor is implemented in 0.35-μm CMOS technology and achieves 10.5 × 10.5 μm pixel size at 29% fill factor. Characterization techniques and measured quantum efficiency, sensitivity, ADC transfer curve, and fixed-pattern noise are presented. A scene with measured dynamic range exceeding 10 000 : 1 is sampled nine times to obtain an image with dynamic range of 65 536 : 1. Limits on achievable dynamic range using multiple sampling are presented.**

***Index Terms*—Analog-to-digital conversion (ADC), CMOS image sensors, digital cameras, dynamic range, image sensors, mixed analog–digital integrated circuits, pixel-level ADC, video cameras.**

I. Introduction

DYNAMIC range for an image sensor, commonly defined as the ratio of its largest nonsaturating signal to the standard deviation of the noise under dark conditions, is often regarded as synonymous to its quality. Since a sensor with higher dynamic can detect a wider range of scene illumination than one with lower dynamic range, it can produce images with greater detail, if not greater quality.

Image sensor dynamic range is often not wide enough to capture the desired scene illumination range. This is especially the case for CMOS image sensors, which, in general, suffer from higher readout noise than charge-coupled devices (CCD's). To enhance the dynamic range of CMOS image sensors, several approaches have been proposed. In [1], the dynamic range of a CMOS active pixel sensor (APS) is enhanced by increasing well capacity one or more times during exposure[1] time using a lateral overflow gate. This results in a compression of the sensor illumination to charge transfer curve [2], [3]. Another approach that achieves consistently higher signal-to-noise ratio (SNR) is multiple sampling [4]. Here a scene is imaged several times at different exposure times, and the images are used to synthesize a high dynamic range image. For this approach to work at reasonable capture times, readout must be performed at speeds much higher than normal APS speeds. In [5], an APS with two column parallel signal chains is presented. The sensor can simultaneously read out two images, one after a short exposure time T and the other after a much longer exposure time, e.g., $32T$. Two images, however, may not be sufficient to represent the areas of the scene that are too dark to be captured in the first image and too bright to be captured in the second. It is difficult to extend the scheme to simultaneously capture more than two images, since more column parallel signal chains must be added at considerable area penalty. A third scheme for enhancing dynamic range involves local shuttering [6]. Even though this scheme is conceptually appealing, it requires a large number of transistors per pixel to implement and a considerable amount of postprocessing to reconstruct the image.

For CMOS sensors operating in instantaneous current readout mode [7], [8], a different approach is used. Here, the photocurrent is fed into a device with logarithmic response, e.g., a diode-connected MOS transistor to compress the sensor transfer curve. Although this scheme can achieve very wide dynamic range, the resulting image quality is generally poor due to low SNR [8].

In this paper, we demonstrate, using a 640 × 512 image sensor with a Nyquist-rate pixel-level analog-to-digital converter (ADC) implemented in a 0.35-μm CMOS technology, that a pixel-level ADC enables a highly flexible and efficient implementation of multiple sampling. Since pixel values are available to the ADC's at all times, the number and timing of the samples as well as the number of bits obtained from each sample can be freely selected without the long readout time of APS. Typically, hundreds of nanoseconds of settling time per row are required for APS readout. In contrast, using a pixel-level ADC, digital data are read out at fast SRAM speeds. This demonstrates yet another fundamental advantage of pixel-level ADC [9] in addition to achieving higher SNR and lower power consumption than column or chip-level ADC approaches—the ability to programmably widen dynamic range with no loss in SNR.

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[1] In this paper, we use integration time and exposure time interchangeably.

In particular we consider sampling at exponentially increasing exposure times, T, $2T$, $\ldots$, 2^kT. Each sampled pixel output is digitized to m bits using the pixel-level ADC. The digitized samples for each pixel are combined into an $m+k$ bit binary number with floating-point resolution. The number can be converted to a floating-point number with exponent ranging from zero to k and an m bit mantissa in the usual way. This increases the sensor dynamic range by a factor of 2^k while providing m bits of resolution for each exponent range of illumination. An important advantage of this scheme, over other dynamic range enhancement schemes [1], is that the combined digital output is linear in illumination. This not only provides more information about the scene but also makes it possible to perform color processing in the standard way. Yet another advantage of this scheme is that the sensor output data rate can be significantly reduced. As we demonstrate in Section III, we do not need to output the full m bits from each sample. In fact, if the sensor response is linear, we only need to output a total of $m+k$, which is the minimum required.

The remainder of this paper is organized as follows. In Section II, we present SNR and dynamic range analysis results [4], which demonstrate the advantage of multiple sampling over the well capacity adjusting scheme. In Section III, we describe the implementation of multiple sampling in a CMOS image sensor with our recently developed pixel-level multichannel bit-serial (MCBS) ADC [9]. In Section IV, we describe the design and operation of a 640×512 image sensor with pixel-level MCBS ADC implemented in a standard digital 0.35-μm CMOS process. In Section V, we describe how we characterized the sensor and present the measured quantum efficiency (QE), sensitivity, ADC transfer characteristics, and fixed pattern noise (FPN). In Section VI, we present a multiple sampling example, where a scene with measured dynamic range exceeding 10 000 : 1 is sampled nine times at exponentially increasing exposure times to obtain a 16-bit image with floating-point resolution. We discuss the limits on achievable dynamic range using multiple sampling.

II. Analysis of SNR for Image Sensors with Enhanced Dynamic Range

The purpose of this section is to motivate the use of multiple sampling to enhance an image sensor dynamic range. We do so by showing that using multiple sampling dynamic range can be enhanced without adversely affecting SNR. This is in contrast to using well capacity adjusting to enhance dynamic range. In this case, increasing dynamic range comes at the expense of potentially unacceptable reduction in SNR.

In [4], we analyzed the SNR and dynamic range for CCD and CMOS image sensors that operate in the integration mode with and without enhanced dynamic range using the model depicted in Fig. 1. The model expresses the output charge Q from a pixel as a function of the photogenerated signal $i_{\rm ph} \geq 0$, dark current $i_d \geq 0$, and noise N, which is the sum of integrated shot noise Q_s and read noise Q_r. Transfer function f_0 describes the relationship between the photodetector current i and the output charge (not including noise).

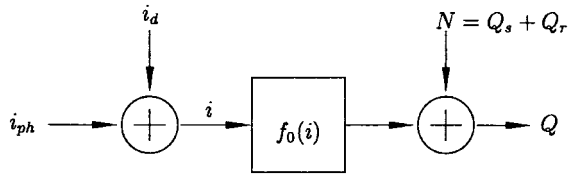


Fig. 1. Sensor model.

To illustrate how this model is used to analyze dynamic range and SNR, we first analyze SNR and dynamic range for a sensor operated in the conventional current integration mode. In the following two subsections, we analyze dynamic range and SNR for the well capacity adjusting and multiple sampling schemes. In Section II-C, we compare the two schemes.

In integration mode, $f_0(i)$ is simply $\min\{it_{\rm int}, q_{\rm max}\}$, where $q_{\rm max} > 0$ is the maximum well capacity. This is plotted in Fig. 2.

Dynamic range is the ratio of the sensor's largest nonsaturating input signal, i.e., input signal swing, to its smallest detectable input signal. The input signal in our case is the photocurrent $i_{\rm ph}$. For integration time $t_{\rm int}$, the largest nonsaturating input signal is given by $i_{\rm max} = (q_{\rm max}/t_{\rm int}) - i_d$. The smallest detectable signal, $i_{\rm min}$, is not as well defined. Clearly, it must be large enough so that it can be discriminated from $i_{\rm ph} = 0$. The convention, which is very optimistic, is to assume that $i_{\rm min}$ is equal to the standard deviation of the input-referred noise when no signal is present.

For i sufficiently below $q_{\rm max}/t_{\rm int}$, the integrated shot noise Q_s has zero mean and variance $q(i_{\rm ph} + i_d)t_{\rm int}$. Since Q_s and Q_r are uncorrelated, the total average noise power $\sigma_Q^2 = q(i_{\rm ph} + i_d)t_{\rm int} + \sigma_r^2$. To find the equivalent zero mean input-referred noise N_i, we redraw the model as shown in Fig. 3. We assume that σ_{N_i} is very small compared to the signal i, and therefore $f_0(i + N_i) \approx f_0(i) + N_i f_0'(i)$ evaluated at i (in mean square), provided the derivative exists. Thus, the average power of the equivalent input-referred noise

$$\sigma_{N_i}^2 = \frac{\sigma_Q^2}{f_0'(i)^2} = \frac{\sigma_Q^2}{t_{\rm int}^2}.$$

Setting $i_{\rm ph}$ to zero, we get $i_{\rm min} = 1/t_{\rm int}\sqrt{qi_dt_{\rm int} + \sigma_r^2}$, and the sensor dynamic range

$$\mathrm{DR} = \frac{i_{\rm max}}{i_{\rm min}} = \frac{q_{\rm max} - i_dt_{\rm int}}{\sqrt{qi_dt_{\rm int} + \sigma_r^2}}.$$

We define the $\mathrm{SNR}(i_{\rm ph})$, which is a function of $i_{\rm ph}$, as the ratio of the input signal power $i_{\rm ph}^2$ to the average input-referred noise power $\sigma_{N_i}^2$. For the sensor in integration mode, we get

$$\mathrm{SNR}(i_{\rm ph}) = \frac{(i_{\rm ph}t_{\rm int})^2}{q(i_{\rm ph} + i_d)t_{\rm int} + \sigma_r^2}, \qquad \text{for } i_{\rm ph} \leq i_{\rm max}.$$

This is plotted in Fig. 4 for a sensor with $q_{\rm max} = 1.25 \times 10^5$ electrons, $\sigma_r = 20$ electrons, and integration time $t_{\rm int} = 30$ ms for three different dark currents $i_d = 1$, 5, and 15 fA. Note that even though the average noise power increases with

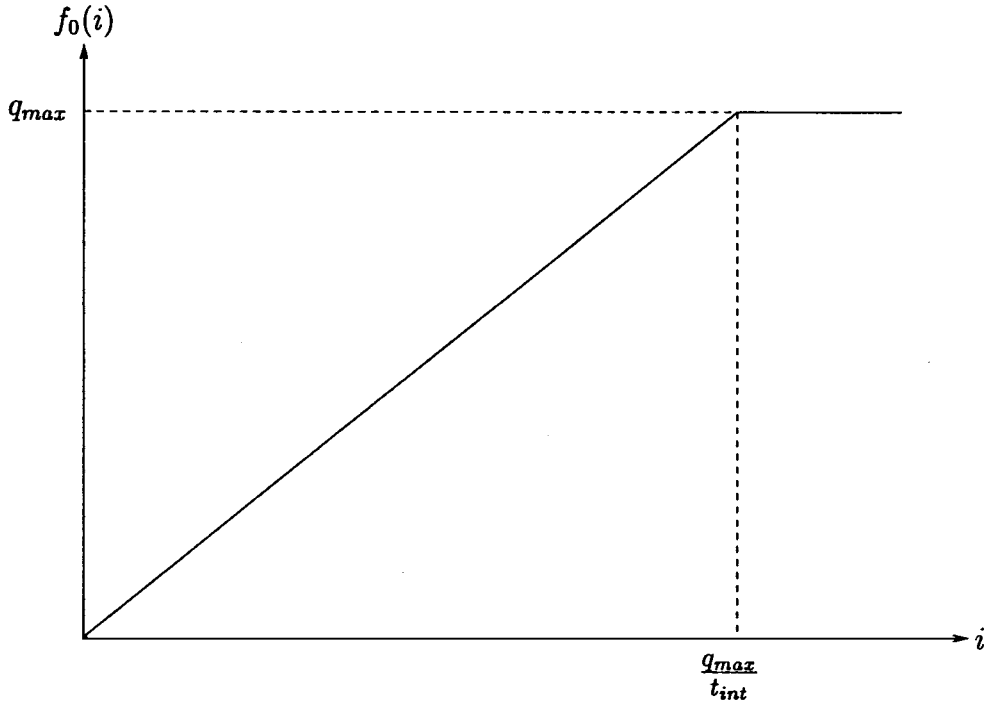


Fig. 2. $f_0(i)$ versus i in integration mode.

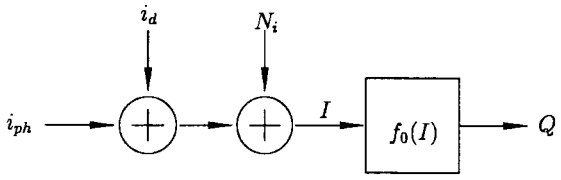


Fig. 3. Sensor model with input-referred noise.

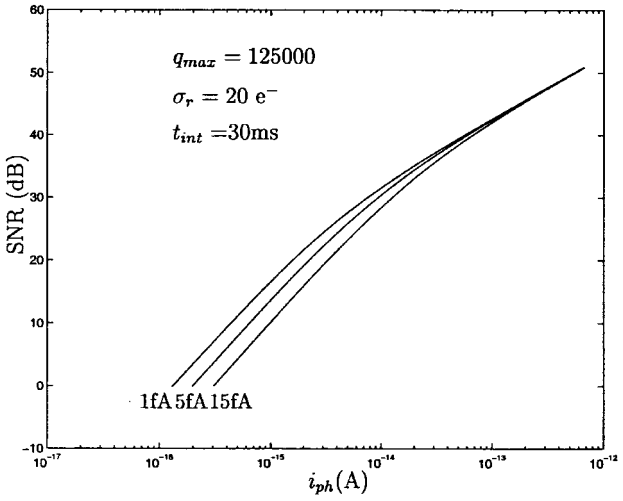


Fig. 4. SNR versus $i_{\rm ph}$.

$i_{\rm ph}$, SNR monotonically increases, first at a rate of 20 dBs per decade when read noise dominates, and ultimately at 10 dBs per decade as shot noise dominates. Also note that the sensor with the highest dynamic range, i.e., the one corresponding to $i_d = 1$ fA, is also the one with the highest SNR. Thus, if we consider SNR to be a good measure of image quality,

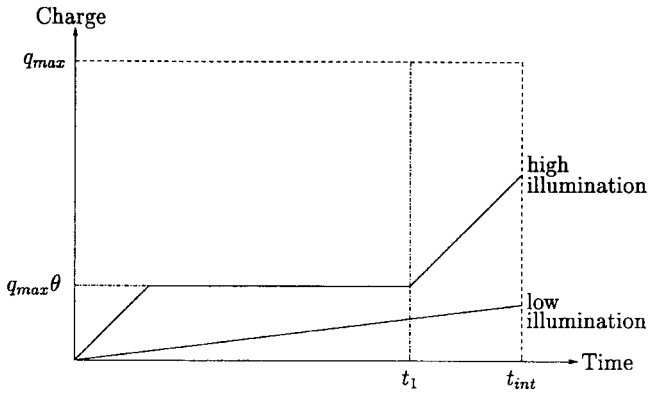


Fig. 5. Charge versus time for well capacity adjusting scheme.

high dynamic range, which is a single number, can be equally regarded as a good measure of quality. This is, however, not necessarily the case when dynamic range enhancement schemes are employed, as we will show in the following subsections.

A. SNR for the Well Capacity Adjusting Scheme

The well capacity adjusting scheme described by Knight [2] and Sayag [3] and implemented by Decker [1] compresses the sensor's current versus charge response curve using a lateral overflow gate, e.g., the reset transistor gate in a CMOS APS. The voltage applied to the overflow gate determines the well capacity. During integration, well capacity is monotonically increased to its maximum value. The excess photogenerated charge is drained via the overflow gate. For example, assume that well capacity is adjusted only once at time t_1 from $q_{\max}\theta$ to full capacity $q_{\max}$. Fig. 5 plots the average collected charge

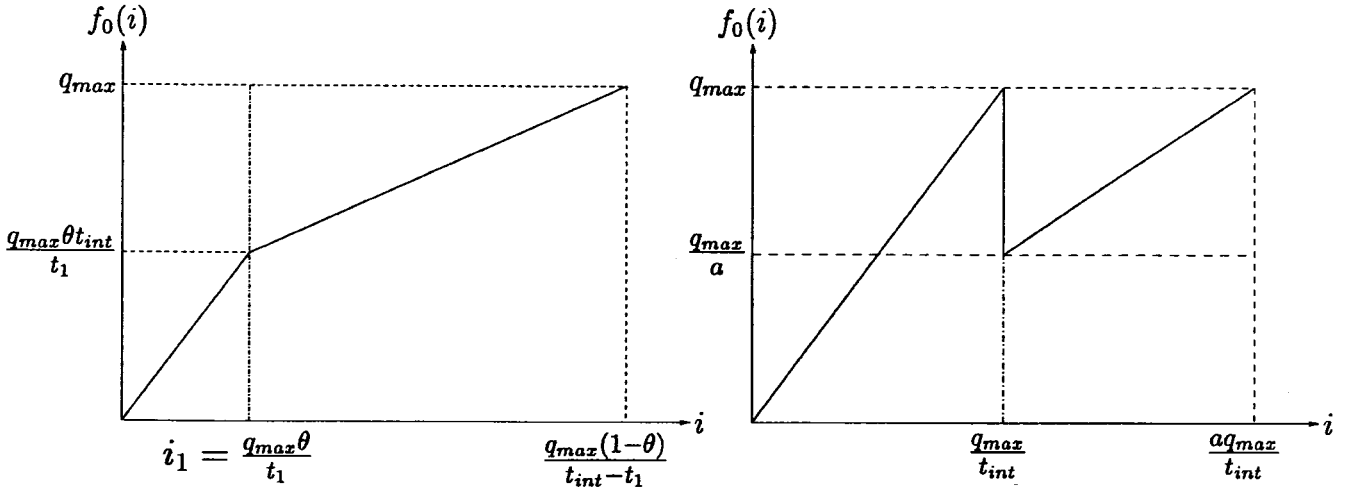


Fig. 6. $f_0(i)$ versus i for (a) well adjusting and (b) dual sampling.

versus time for two input photocurrent values. Note that when the collected charge reaches $q_{\max}\theta$, e.g., the high illumination case in the figure, the output charge is clipped until time t_1.

In this case the relationship between i and Q is plotted in Fig. 6(a). Note that the slope decreases beyond $i = i_1 = q_{\max}\theta/t_1$, which results in the compression of the response.

In order to compute SNR and dynamic range, we need to compute the input-referred noise power σ_Q^2. It is important to note that the input-referred noise power is not simply $\sigma_Q^2/t_{\text{int}}^2$ since the relationship between i and Q is nonlinear.

It can be easily shown that

$$\text{SNR}(i_{\text{ph}}) = \begin{cases} \dfrac{i_{\text{ph}}^2 t_{\text{int}}^2}{q(i_{\text{ph}}+i_d)t_{\text{int}}+\sigma_r^2}, \\ \quad \text{if } 0 \le i_{\text{ph}} < \dfrac{q_{\max}\theta}{t_1} - i_d \\ \dfrac{i_{\text{ph}}^2 (t_{\text{int}}-t_1)^2}{q(i_{\text{ph}}+i_d)(t_{\text{int}}-t_1)+\sigma_r^2}, \\ \quad \text{if } \dfrac{q_{max}\theta}{t_1} - i_d \le i_{\text{ph}} < \dfrac{q_{\max}(1-\theta)}{t_{\text{int}}-t_1} - i_d. \end{cases}$$

Now, $i_{\max} = (q_{\max}(1-\theta)/t_{\text{int}} - t_1) - i_d$, and $i_{\min}$ is the same as before. Thus, for small i_d, dynamic range is enhanced by a factor

$$\text{DRF} = \frac{1-\theta}{1-\dfrac{t_1}{t_{\text{int}}}}.$$

At i_1, assuming that shot noise dominates, $\text{SNR}(i_{\text{ph}})$ dips by a factor

$$\text{DIP} = \left(1 - \frac{t_1}{t_{\text{int}}}\right)$$

which is inversely proportional to the dynamic range enhancement factor (DRF). This is illustrated in Fig. 7, where SNR is

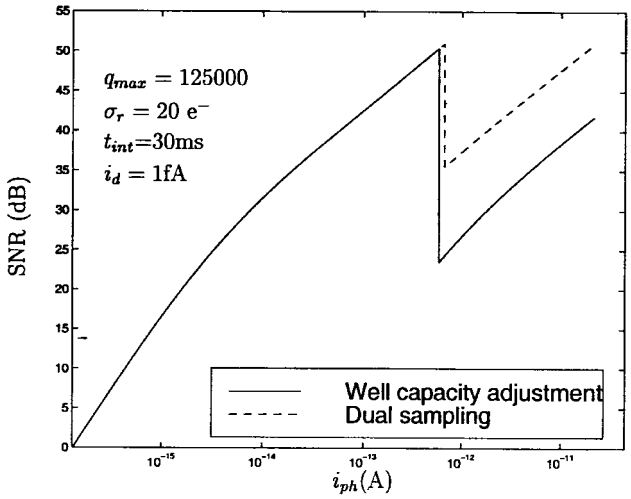


Fig. 7. SNR versus i_{ph} for both well capacity adjusting (solid line) and dual sampling (dotted line). DRF = 32.

plotted versus i_{ph} using the same sensor parameters as before and assuming that $i_d = 1$ fA, $\theta = 7/8$, and $t_1/t_{\text{int}} = 255/256$. In this case, DRF ≈ 32 and DIP $\approx 1/256$, i.e., around 24 dBs. The DIP poses a theoretical limit on how much dynamic range can be enhanced via this method since the dip can become so large that SNR reaches close to 0 dB in the middle, making the concept of dynamic range very misleading.

The analysis can be extended to any number of well capacity adjustments k. In this case, let $0 < \theta_i < 1$, $1 \le i \le k$, be the resulting fractions of the well capacity corresponding to the adjustments and $0 < t_i < t_{\text{int}}$ be the adjustment times. It can be shown that dynamic range expands by

$$\text{DRF} = \frac{\dfrac{q_{\max}(1-\theta_k)}{t_{\text{int}}-t_k} - i_d}{\dfrac{q_{\max}}{t_{\text{int}}} - i_d} \approx \frac{1-\theta_k}{1-\dfrac{t_k}{t_{\text{int}}}}.$$

It can be shown that as dynamic range is increased, the final $\text{SNR}(i_{\max})$ degrades by the same factor $1-\theta_k$ relative

to peak SNR when no dynamic range enhancement is used. Moreover, the sum of the SNR dips, expressed in dB's, is approximately $|10\log_{10}(1-t_k/t_{\rm int})|$, which is always greater than DRF expressed in dB's.

B. SNR for the Multiple Sampling Scheme

Dual sampling has been used to enhance the dynamic range for CCD sensors, charge modulation device (CMD) sensors [10], and CMOS APS sensors [11]. A scene is imaged twice, once after a short integration time and again after a much longer integration time, and the two images are combined into a high dynamic range image. Conceptually, the short integration time image captures the high illumination areas before the well saturates, and the long integration time image captures the low illumination areas after adequate integration time.

To analyze dynamic range and SNR for dual sampling, we again use our simple model. We consider sampling at $t_{\rm int}/a$ and $t_{\rm int}$, for $a > 1$. Fig. 6(b) plots $f_0(i)$ versus i for dual sampling. Note that, unlike the previous two cases, $f_0(\cdot)$ is not a one-to-one function.

It is easy to compute

$$\mathrm{SNR}(i_{\rm ph}) = \begin{cases} \dfrac{i_{\rm ph}^2 t_{\rm int}^2}{q(i_{\rm ph}+i_d)t_{\rm int}+\sigma_r^2}, \\ \quad \text{if } 0 \le i_{\rm ph} < \dfrac{q_{\rm max}\theta}{t_{\rm int}} - i_d \\ \dfrac{i_{\rm ph}^2 (t_{\rm int}-t_1)^2}{q(i_{\rm ph}+i_d)(t_{\rm int}-t_1)+\sigma_r^2}, \\ \quad \text{if } \dfrac{q_{max}\theta}{t_1} - i_d \le i_{\rm ph} < \dfrac{q_{\rm max}(1-\theta)}{t_{\rm int}-t_1} - i_d. \end{cases}$$

Since $i_{\rm max} = aq_{\rm max}/t_{\rm int} - i_d$ and $i_{\rm min}$ is the same as before, the dynamic range enhancement factor

$$\mathrm{DRF} = \frac{\dfrac{aq_{\rm max}}{t_{\rm int}} - i_d}{\dfrac{q_{\rm max}}{t_{\rm int}} - i_d} \approx a, \text{ for small } i_d.$$

As in the case of well capacity adjusting, SNR dips in the middle. For the same DRF, however, the dip is smaller. Moreover, the final SNR $(i_{\rm max})$ is always equal to the peak SNR without dynamic range enhancement.

Fig. 7 plots SNR versus $i_{\rm ph}$ for $a = 32$, $t_{\rm int} = 30$ ms and assuming the same sensor parameter values as before.

The analysis can be extended to multiple sampling in general. For $k+1$ samples at $t_{\rm int}/2^k$, $t_{\rm int}/2^{k-1}$, …, $t_{\rm int}/2$, $t_{\rm int}$), we get

$$\mathrm{DRF} = \frac{\dfrac{2^k q_{\rm max}}{t_{\rm int}} - i_d}{\dfrac{q_{\rm max}}{t_{\rm int}} - i_d} \approx 2^k.$$

C. Multiple Sampling Versus Well Capacity Adjusting

We have shown that using the well adjusting scheme, SNR degrades as dynamic range is increased. On the other hand, using the multiple sampling scheme, dynamic range can be widened without degrading SNR. Intuitively, multiple sampling achieves better SNR because the effective well capacity is essentially the full well capacity independent of illumination level, whereas for the well adjusting scheme, the effective well capacity decreases as illumination level increases. For the example in Section II-A [Fig. 6(a)], for $i > (q_{\rm max}\theta/t_1)$, the effective well capacity is only $q_{\rm max}(1-\theta)$. To demonstrate this, in Fig. 8 we plot SNR versus $i_{\rm ph}$ for both well capacity adjusting and for multiple sampling assuming $k = 8$, $t_{\rm int} = 30$ ms, and the same sensor parameter values as before. In the well capacity adjusting case, the capacity levels $\theta_i = i/10$ and adjustment times $t_i = 1 - 1/10 * 2^{i-1}$ for $i = 1, 2, \ldots, 8$ are chosen so that the resulting average charge $f_0(\cdot)$ versus $i_{\rm ph}$ curve assumes an *A-law* companding shape. The sum of the SNR dips is ≈ 31 dBs, and SNR$(i_{\rm max})$ degrades by 7 dB. Both schemes achieve DRF = 256. Note that multiple sampling achieves around 10 dB higher SNR. Moreover, SNR for the well adjusting scheme dips by more than 10 dB in the middle. This clearly demonstrates that multiple sampling enjoys better SNR than well capacity adjustment at the same DRF. In fact, if we include fixed pattern noise, well barrier thermal noise, and quantization noise in our analysis, it can be shown that the difference in SNR in favor of multiple sampling is even greater.

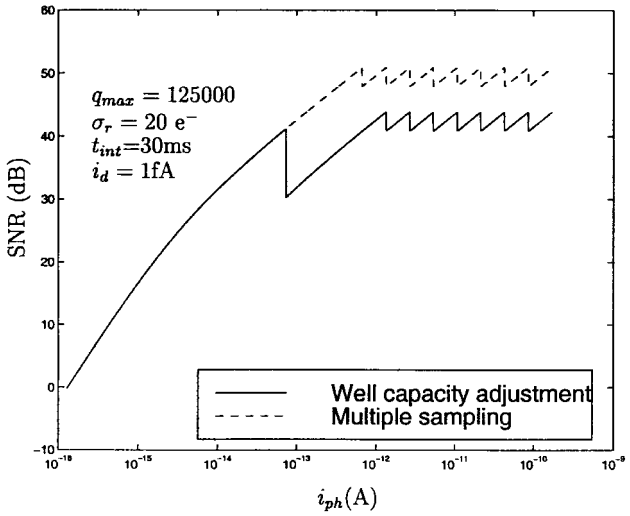


Fig. 8. SNR versus $i_{\rm ph}$ for both well capacity adjusting (solid line) and multiple sampling (dotted line). DFR = 256.

III. Multiple Sampling Using Image Sensor with Pixel-Level MCBS ADC

In this section, we describe how pixel-level MCBS ADC enables a flexible and programmable implementation of multiple sampling to enhance dynamic range. In the following section, we describe the implementation of a 640 × 512 CMOS image sensor with the pixel-level MCBS ADC.

The operation of the MCBS ADC is described in detail in [9]. The ADC is bit serial, and each bit is generated by performing a set of comparisons between the pixel values and a monotonically increasing staircase RAMP signal. The bits can be generated in any order and independent of other bits. Data are read out of the image sensor in bit planes instead

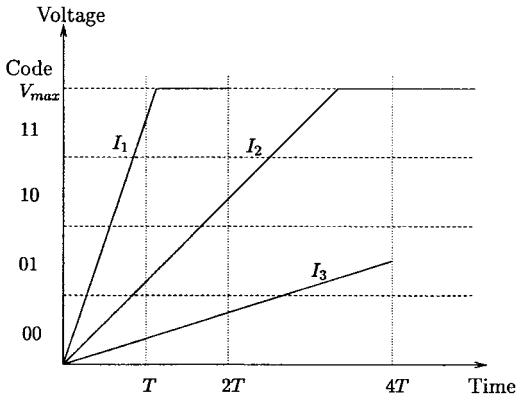


Fig. 9. Pixel output voltage and its digitized value versus time.

of the conventional raster-scan format. Each ADC channel is implemented using only a 1-bit comparator and a 1-bit latch. The signals required to operate the ADC's are globally generated and shared by all channels.

An image sensor with pixel-level MCBS ADC can implement multiple sampling in a very general manner. Since the signals are available to the ADC's at all times and all ADC's operate in parallel, the number of samples, exposure times, and the number of bits read out from each sample can be freely chosen. Here, we consider the implementation of multiple sampling using exponentially increasing exposure times $T, 2T, 4T, \ldots, 2^kT$. Each sample pixel output is digitized to m bits. The digitized samples for each pixel are combined into an $m+k$ bit binary number with floating-point resolution. The number can be converted to a floating-point number with exponent ranging from zero to k and an m-bit mantissa in the usual way. This increases the sensor dynamic range by a factor of 2^k, while providing m bits of resolution for each exponent range of illumination.

The m bit samples from each pixel can be combined into an $m+k$ bit number by simply scaling the last m bit sample before the pixel saturates by a factor of 2^{k+1-l}, where $1 \le l \le k+1$ is the sample index. We do not, however, need to output all of the m bits from each sample. In fact, if the sensor photon to output voltage response is linear, only a total of $m+k$ bits, which is the minimum required number of bits, need to be read out from the k samples.

To illustrate how we save bits during readout, consider an example with $k = 2$ and $m = 2$, i.e., where we sample a scene three times at T, $2T$, and $4T$ and digitize each sample to 2 bits of resolution. Fig. 9 plots the output pixel voltage versus time for three constant illuminations I_1, I_2, and I_3, assuming linear photon to voltage response, and saturation voltage $V_{\max}$. The voltage is sampled after exposure times T, $2T$, and $4T$. Each sample is digitized to 2 bits using binary code as shown in the figure. The first sample is digitized to x_1x_2, e.g., 11 for I_1. The second is also digitized to 2 bits. Since the second sample is twice the value of the first, the 2 bits are x_2x_3 if the sample is not saturated, i.e., $< V_{\max}$, and 11 if it is. In either case, the ADC only needs to generate the least significant bit x_3. Similarly, for the third sample at $4T$, only the least significant bit x_4 needs to be generated. Table I lists the bit values for each illumination and the corresponding binary floating-point representation. This scheme can be easily extended to any exponent k and mantissa m. The first sample is digitized to m bits; then only the least significant bit is generated from each consecutive sample, and they are simply appended to the first sample during decimation. Thus, as long as the sensor photon to voltage response is linear, only $m+k$ bits need to be read out, which is the minimum required. This further reduces readout time. Often more bits need to be read out from the samples to correct for sensor nonlinearity, offset, and noise.

TABLE I
DIGITIZED VALUES FOR THREE ILLUMINATION LEVELS

Illumination	$x_1x_2x_3x_4$	Exponent	Mantissa
I_1	1 1 1 1	2	11
I_2	0 1 0 1	1	10
I_3	0 0 0 1	0	01

TABLE II
QUANTIZATION TABLE FOR THE $m = 2$, $k = 2$ EXAMPLE USING A GRAY CODE. EACH GRAY CODEWORD IS FIRST DECODED INTO A BINARY NUMBER AND THEN REPRESENTED BY A FLOATING-POINT NUMBER. THE ILLUMINATION IS MEASURED AS THE VOLTAGE AT T, ASSUMING $V_{\max} = 1$. NOTE THAT DIGITAL DYNAMIC RANGE HAS INCREASED FROM 4:1 TO 16:1

Ilumination Range	$x_1x_2x_3x_4$	Binary number	DN	Exponent	Mantissa
$0 - \frac{1}{16}$	0 0 0 0	0 0 0 0	0	0	0 0
$\frac{1}{16} - \frac{2}{16}$	0 0 0 1	0 0 0 1	1	0	0 1
$\frac{2}{16} - \frac{3}{16}$	0 0 1 1	0 0 1 0	2	0	1 0
$\frac{3}{16} - \frac{4}{16}$	0 0 1 0	0 0 1 1	3	0	1 1
$\frac{4}{16} - \frac{6}{16}$	0 1 1 1	0 1 0 1	5	1	1 0
$\frac{6}{16} - \frac{8}{16}$	0 1 0 0	0 1 1 1	7	1	1 1
$\frac{8}{16} - \frac{12}{16}$	1 1 1 0	1 0 1 1	11	2	1 0
$\frac{12}{16} - 1$	1 0 0 0	1 1 1 1	15	2	1 1

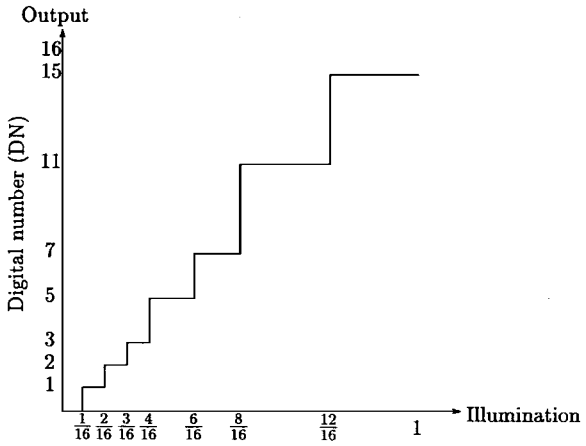


Fig. 10. Illumination to output DN transfer curve corresponding to Table II.

Table II provides the complete quantization table and corresponding illumination to digital number (DN) transfer curve for the $m = 2$ and $k = 2$ example. Note that we use a Gray code instead of the binary code in this case. The transfer curve is plotted in Fig. 10. The exponentially increasing step sizes indicate that the ADC indeed has a floating-point resolution. Note that the ADC output is a linear function of illumination. This is in contrast to schemes such as well capacity adjusting where the response is not linear. One important advantage

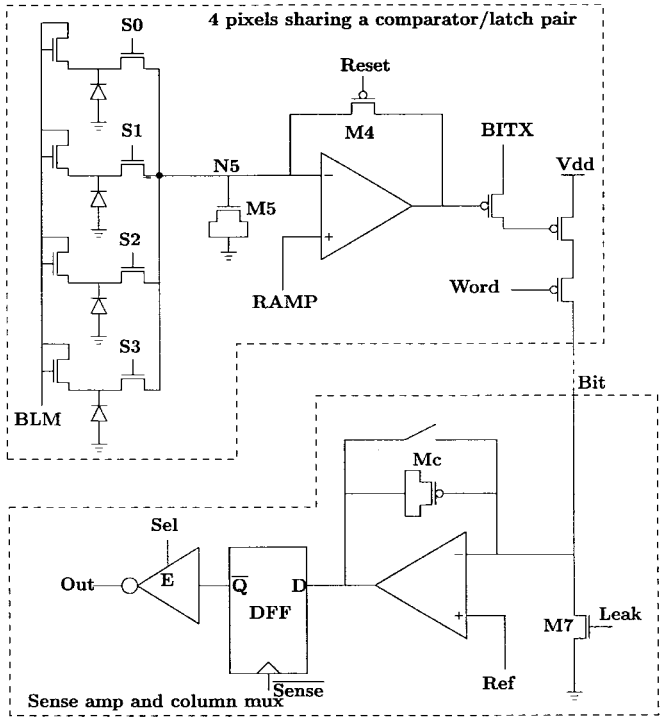


Fig. 11. Pixel block and column sense amplifier circuit.

of linearity is that color processing can be done in the usual way.

IV. A 640 × 512 CMOS Image Sensor

In this section, we describe the circuit design and operation of a 640 × 512 image sensor with pixel-level MCBS ADC implemented in a 0.35-μm standard digital CMOS process.

To achieve acceptably small pixel size, each ADC is multiplexed among four neighboring pixels. A circuit schematic of four pixels sharing an ADC is depicted in Fig. 11. The 1-bit comparator/latch circuit is described in [9]. An antiblooming transistor is connected to each photodetector to avoid blooming during multiple sampling. The four photodetectors are connected to the ADC via an analog multiplexer controlled by S0, S1, S2, and S3. All ADC's still operate in parallel but serve one quarter image at a time, as shown in Fig. 12. Note that there is a timing skew equal to the ADC conversion time between consecutive quarter images. To achieve reasonably small skew, the ADC time is set to equal one-seventeenth of the integration time. As shown in Fig. 12, before A/D conversion is performed, the charge collected by each photodetector is sampled onto a sample/hold (S/H) capacitor M5. After ADC, the S/H capacitor and the photodetector are reset via the Reset signal, which causes the comparator to operate as an op-amp in unity-gain feedback. Autozeroing is performed during reset since the comparator offset voltage is stored on the photodetector capacitance in addition to the reset voltage. This autozeroing feature in effect performs correlated double sampling, which significantly reduces FPN, and $1/f$ noise. The column sense amplifier shown in the figure is designed for high speed, low noise, and power. A charge amplifier is used to minimize bitline voltage swing. To sense the bitline, capacitor Mc is first reset, and the current from the pixel and transistor M7 is integrated. The sensed bit is latched using a flip-flop. The tristate inverter is part of a 10 : 1 mux. The signals required to operate the ADC's including RAMP and BITX are globally generated by off-chip DAC and digital control circuitry.

An essential feature of the sensor design is electrical testability. Since the ADC input (node N5 in Fig. 11) can be reset to any voltage via RAMP, the ADC can be fully tested without any light or optics. To test the ADC, the photodetectors are disconnected by turning off the select transistors. The comparator/latch pair input is then set to the desired RAMP value by turning on M4. The set value is then quantized and read out. By stepping the ADC input through its entire input range, the ADC transfer curve can be obtained without any light or optics. This not only greatly simplifies testing of the ADC itself but also makes characterizing the image sensor easier, since the only remaining unknown parameters are the photodetector and the S/H capacitances.

A photomicrograph of the image sensor chip is provided in Fig. 13. The main chip characteristics are summarized in Table III.

V. Characterization of the 640 × 512 Image Sensor

In [12], we described techniques for characterizing image sensors with Nyquist-rate pixel-level ADC. In this section, we briefly review this work and provide the characterization results for our 640 × 512 image sensor.

Techniques for characterizing CCD image sensors have been developed over many years. An excellent description of these techniques is provided by Janesick [13]. His paper describes the CCD transfer concept and how it is used to characterize such parameters as charge transfer efficiency, QE, linearity, gain, offset, signal-to-noise, nonuniformity, dynamic range, and mean time to failure. Since the signal path for CMOS image sensors is quite different from CCD's, the CCD characterization models and techniques cannot be directly used for their characterization. In [14], we extended the Janesick method to CMOS APS. The modifications account for the nonlinearity, pixel gain variations, and read noise of APS. In [15], we modeled APS FPN as an outcome of the sum of two uncorrelated components, a column component, and a pixel component. The paper shows how the model parameters are estimated from measurements of the image sensor outputs under uniform illumination.

Characterizing CMOS image sensors with pixel-level ADC is quite challenging. The method in [14] cannot be used since it relies on estimating shot noise statistics, which requires digitizing pixel output values to 12 or more bits of resolution. Our image sensor provides no facility for directly reading out the analog pixel values before ADC is performed, and the ADC resolution is limited to a maximum of 8 bits. The electrical testability feature described in Section IV can be used to alleviate this problem, however.

In the next subsection, we describe how we characterize the sensor signal path, and provide measured results. In Section V-B, we present an FPN model suited for our image sensor

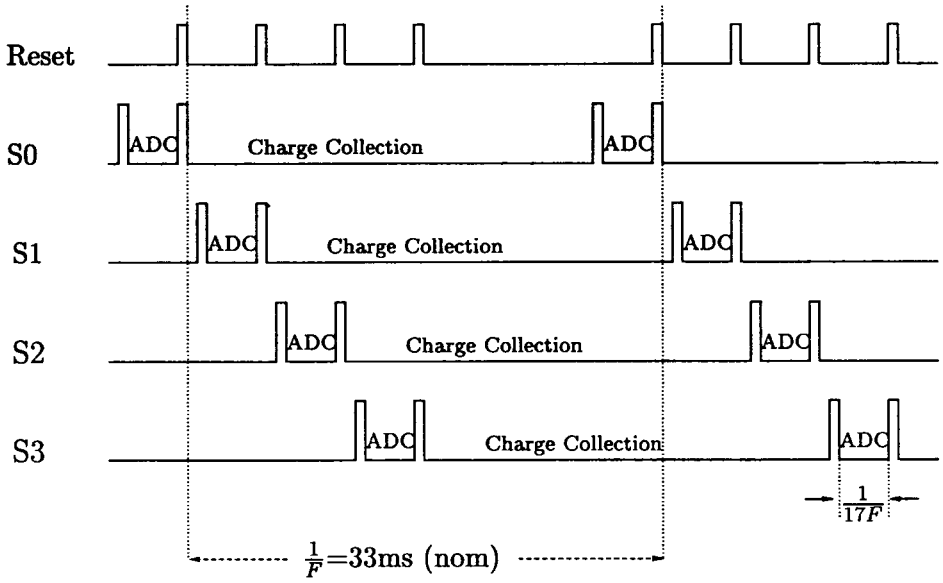


Fig. 12. A frame consists of four staggered quarter frames.

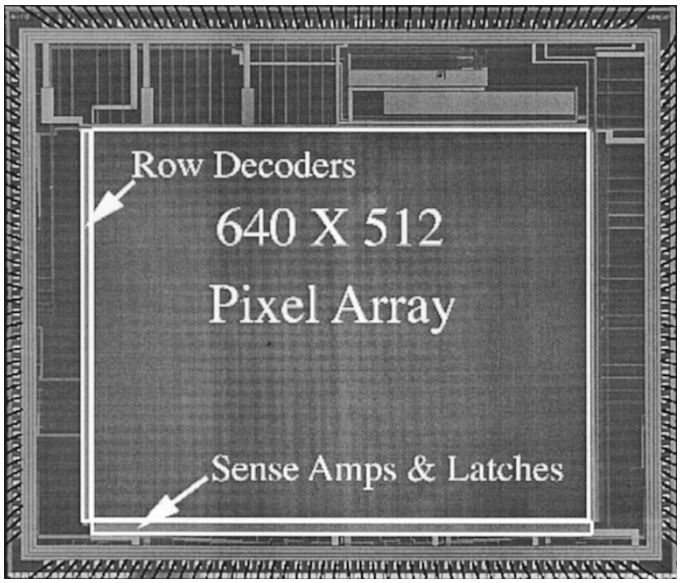


Fig. 13. Die micrograph of 640 × 512 image sensor.

TABLE III
MAIN CHARACTERISTICS OF 640 × 512 AREA IMAGE SENSOR

Technology	0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS
Sensor size	640 × 512 pixels
Pixel size	10.5 μm × 10.5 μm
Photodetector	n-well to p-sub diode
Sensor area	6720 μm × 5376 μm
Fill factor	29%
Transistors per pixel	5.5 (22 per four pixels)
Package	180 pin PGA
Supply voltage	3.3V
Sensor power consumption	80 mW
Signal swing	0.5–2.5V
Maximum frame rate	250 frames/s (@ 8-bit resolution)
Dark current	1.3 mV/sec (160 pA/cm^2) at 25°C

architecture and provide estimates of the model parameters from measurements of the sensor.

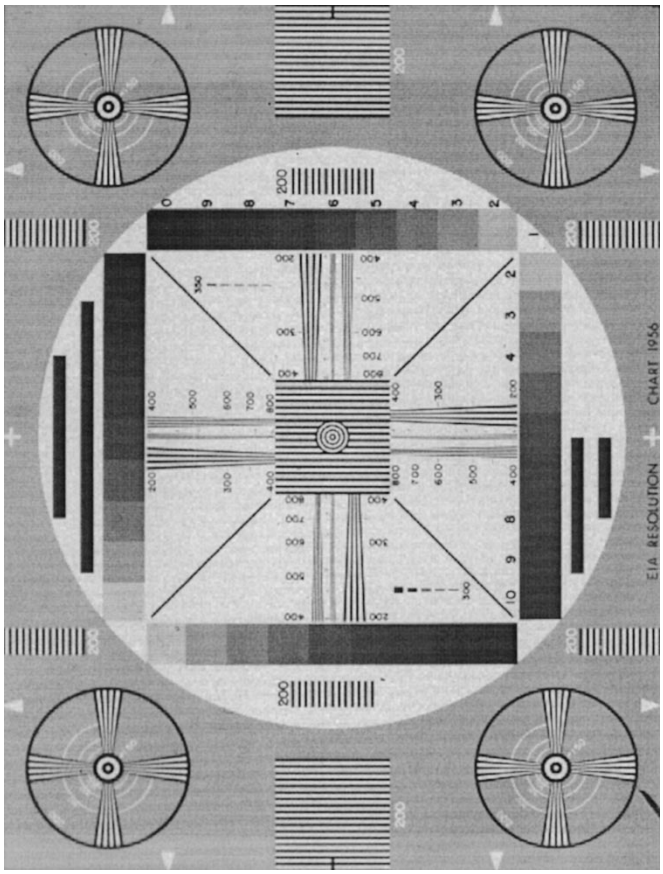


Fig. 14. A 640 × 512 image of the EIA 1956 resolution chart (uncorrected and unprocessed).

A. Signal Transfer Characteristics

A description of the experimental setup we used to characterize our image sensor is provided in [9] and will not be repeated here. The image sensor is fully functional, and we are able to obtain high-quality images using our setup. Fig. 14 is

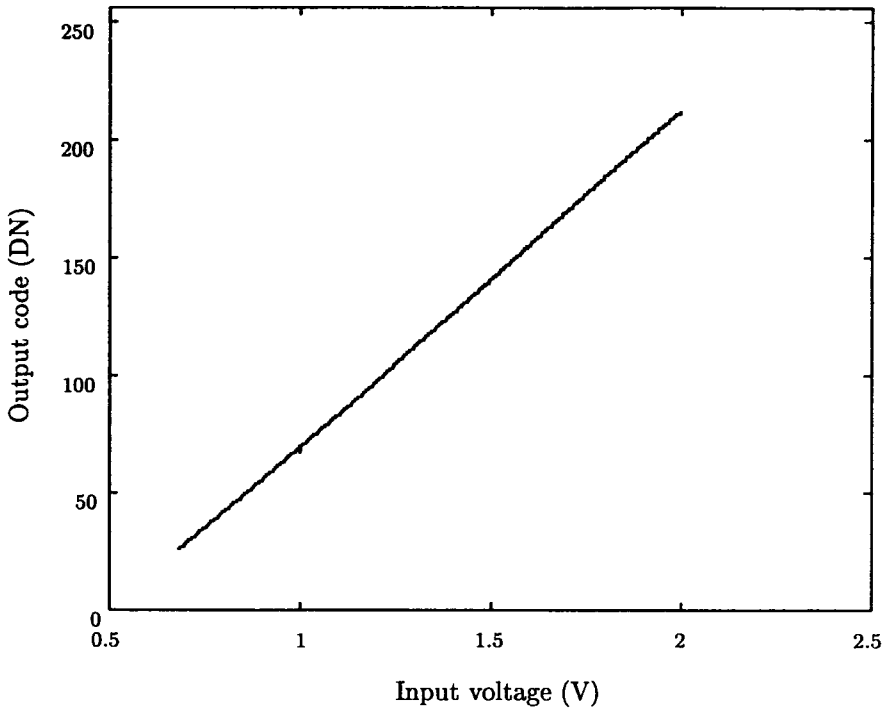


Fig. 15. Measured ADC transfer curve.

an 8-bit image of the EIA 1956 resolution chart obtained from our image sensor. The image was not corrected or processed before printing.

To measure the photon to DN transfer curve, we irradiated the image sensor with constant monochromatic illumination at 610 nm. To find the transfer curve, we varied integration time rather than illumination. We read out the image sensor DN output after 21 linearly increasing integration times 7, 33, 59, ..., 534 ms. The experiment was repeated 256 times, and the results were averaged to remove temporal noise. The averaged transfer curve is quite linear. Therefore, we can simply express the signal path gain G_1 (DN/ph) as the product of QE (e^-/ph), sensitivity (V/e^-), and ADC gain G_{ADC} (DN/V). In theory, the ADC gain is entirely determined by the DAC and is equal to 256 divided by the DAC's input signal swing. The measured DAC's input swing is 2 V, and its transfer curve shows 16 bits of linearity. Therefore, $G_{\mathrm{ADC}} = 128$DN/V. In practice, however, we must verify that the ADC is linear. To do so, we used the electrical testability feature described in Section IV to obtain the ADC transfer curve shown in Fig. 15. Note that it is quite linear and that its slope is 136 (DN/V). The discrepancy between the true $G_{\mathrm{ADC}} = 128$DN/V and the measured ADC gain using electrical testing, which is 136, stems from the fact that during electrical testing, resetting introduces charge injection error that is proportional to the reset value. This makes the gain of the measured ADC transfer curve larger than its true value. This effect was verified by switching the select signals to inject varying amounts of charge and observing that the gain varies accordingly.

To estimate QE, we need to know the sensor sensitivity. Existing techniques [13], [14] estimate sensitivity using shot noise statistics. For these techniques to work, the pixel values need to be quantized to at least 12 bits so that quantization noise is significantly lower than shot noise. Our pixel-level ADC produces only 8 bits, and it would be difficult to extend its resolution to the needed 12 bits or higher.[2] However, since we already know the ADC transfer curve, the only unknown factor needed to determine sensitivity is the sense node capacitance, which is the sum of the capacitance of the photodetector and its parasitics C_d, and the S/H capacitor and its parasitics $C_{\mathrm{S/H}}$ (see Fig. 11). Using the provided process data, we estimated the sample/hold capacitance, which is the gate capacitance of M5, to be 22.6 fF and its parasitics to be around 2 fF. Thus $C_{\mathrm{S/H}}$ is estimated at 24.6 fF. Since we used an n-well/p-sub photodiode, no process data were available to us. Fortunately, we were able to estimate the ratio of the two capacitances $C_d/C_{\mathrm{S/H}}$ experimentally as follows.

We ganged up two photodiodes, by simultaneously turning on S0 and S1, and obtained the signal transfer curve and its corresponding signal path gain G_2. We repeated the experiment by ganging up three photodiodes and then all four photodiodes to obtain the corresponding signal path gains G_3 and G_4. Using the linear capacitor charge to voltage relation, we get the four relations $(iC_d + C_{\mathrm{S/H}})G_i = k$, for $i = 1$, 2, 3, and 4, where $k = qQE \times G_{\mathrm{ADC}}$. We used least squares to estimate the two unknowns $C_d/C_{S/H}$ and k. The estimate of $C_d/C_{\mathrm{S/H}}$ was 0.275, which gives an estimate of the total sense node capacitance $C_d + C_{\mathrm{S/H}}$ of 31.37 fF and an estimate of the sensitivity of 5.1 μV/e^-.

Dividing signal path gain G_1 by the product of the estimates of sensitivity and G_{ADC}, we found that $QE = 3.23\%$. Since only 29% of the pixel is exposed to light while the rest is

[2] Our ADC resolution depends on the comparator gain. In our image sensor, the gain is not large enough to support 12 bits or higher. Comparator gain can be increased by adding another stage, i.e., an inverter.

TABLE IV
MEASURED PARAMETERS OF THE IMAGE SENSOR

Pixel size	$10.5\,\mu m \times 10.5\,\mu m$
Fill Factor	29%
Photodetector area	7.8% of a pixel
Photodetector capacitance	6.8 fF
Sample and hold capacitance	24.6fF
Signal path gain	2.09×10^{-5} DN/ph
Sensitivity	$5.1\ \mu V/e^-$
ADC gain	128 DN/V
Quantum efficiency	11.3% for exposed area and 42% for detector area @ 610 nm

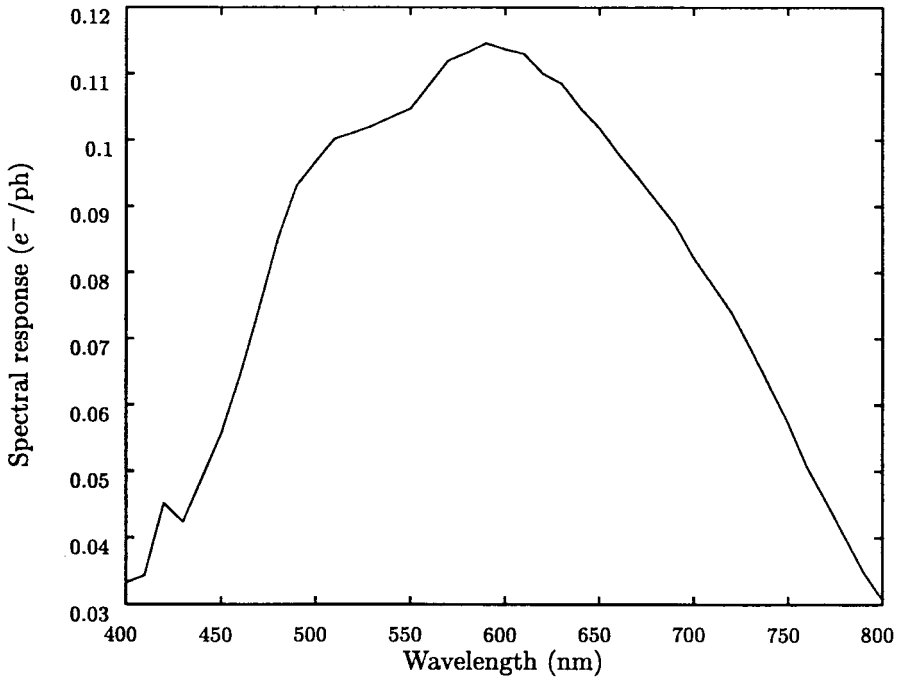


Fig. 16. Measured average spectral response of the image sensor.

covered by a metal shield, QE relative to the exposed area is around 11.3%. Moreover, since the photodetector itself occupies[3] only 7.8% of the pixel area, QE relative to the photodetector is 42%.

Table IV summarizes the measured parameters for the 640 $\times$ 512 image sensor.

The spectral response of the image sensor was obtained by repeating the procedure we used to estimate QE at different wavelengths. Fig. 16 plots the measured average spectral response from 400 to 800 nm.

B. Characterizing FPN and Temporal Noise

FPN is the variation in output pixel values, under uniform illumination, due to device and interconnect mismatches across an image sensor. In a CCD image sensor, FPN is only due to variations in the photodetectors, which are uncorrelated and can thus be modeled as a sample from a spatial white noise process. For a CMOS passive pixel sensor (PPS) or APS, there are many more sources of FPN. In [15], we model PPS and APS FPN as the sum of two components: a column and a pixel component. Each component is modeled by a first-order isotropic autoregressive process, and the processes are assumed to be uncorrelated. For our pixel-level ADC image sensors, FPN is due to the variations among the photodetectors and the variations among the ADC's. Photodetector variations are caused not only by the random variations in the photodetectors but also by the systematic variations due to layout asymmetries resulting from multiplexing. Since each block of 2×2 pixels shares an ADC, each quadrant of the image sensor array is completely symmetrically laid out. However, there are very small, unavoidable differences between the quadrant layouts, which cause quadrant output offsets. Following a similar methodology to [15], we model FPN as an outcome of a two-dimensional random process, which is the sum of two uncorrelated processes, one representing the ADC FPN and the other representing the photodetector FPN. For each quadrant, we represent photodetector FPN as an outcome of a white noise process[4] plus a quadrant offset. We assume that the four processes are uncorrelated. We model the FPN due to the

[3] We used an n-well/p-sub photodiode. As a result, much of the exposed area had to be used to satisfy the well spacing rules.

[4] This is supported by results for both CCD FPN and PPS pixel FPN.

TABLE V
ESTIMATED FPN UNDER DARK, 30% AND 78% FULL WELL SIGNAL LEVELS

	Dark	30% full well	78% full well
Quadrant offset Δ_q (DN)	0.0	0.01	-3.89
	0.0	-0.10	0.42
	0.0	0.07	1.61
	0.0	0.04	1.86
photodetector FPN X(DN)	0.0	0.09	2.03
ADC FPN Y (DN)	0.0	0.13	0.06
total FPN F (DN)	0.0	0.22	2.09
a	0.02	0.021	0.028
σ_U^2	0.13	0.126	0.058

ADC's as an outcome of a first-order isotropic autoregressive process.

Mathematically, we represent FPN for pixel (i, j) as

$$F_{i,j} = X_{i,j} + \Delta_q + Y_{\lceil i/2 \rceil, \lceil j/2 \rceil}$$

where q is the quadrant index of the pixel, Δ_q is the quadrant offset, $\{X_{i,j}\}$ is the white noise process representing photodetector FPN, and $\{Y_{\lceil i/2 \rceil, \lceil j/2 \rceil}\}$ is the process representing ADC FPN, which we assume to be a first-order isotropic autoregressive process of the form

$$\begin{aligned} Y_{\lceil i/2 \rceil, \lceil j/2 \rceil} = a(&Y_{\lceil i/2 \rceil - 1, \lceil j/2 \rceil} + Y_{\lceil i/2 \rceil + 1, \lceil j/2 \rceil} \\ &+ Y_{\lceil i/2 \rceil, \lceil j/2 \rceil - 1} + Y_{\lceil i/2 \rceil, \lceil j/2 \rceil + 1}) \\ &+ U_{\lceil i/2 \rceil, \lceil j/2 \rceil} \end{aligned}$$

where the $U_{\lceil i/2 \rceil, \lceil j/2 \rceil}$ are zero mean uncorrelated random variables with the same variance σ_U^2 and $0 \leq a \leq 1/4$ is a parameter that characterizes the dependency of $Y_{\lceil i/2 \rceil, \lceil j/2 \rceil}$ on its four neighbors.

Thus, to characterize FPN for our sensor, we need to estimate the ADC FPN parameters σ_U^2 and a, and the photodetector FPN parameters Δ_q and $\sigma_{X^q}^2$ for the four quadrants. The $F_{i,j}$'s are obtained by reading out the pixel output values multiple times under the same uniform illumination, temporally averaging the values for each pixel to get an averaged pixel value $\overline{V_{i,j}}$, and then subtracting off the overall average pixel output $\overline{V}$ from each $\overline{V_{i,j}}$. Since the ADC's can be directly characterized, the $Y_{\lceil i/2 \rceil, \lceil j/2 \rceil}$'s are obtained by resetting all pixels to $\overline{V}$, reading out the ADC output values multiple times, temporally averaging the values for each ADC, and subtracting off $\overline{V}$. To estimate the model parameters σ_U^2 and a, we first estimate σ_Y^2 and covariance $R_Y(1, 0)$ using the estimators given in [15]. Now we can estimate the photodetector FPN and the quadrant offset as

$$X_{i,j} + \Delta_q = F_{i,j} - Y_{\lceil i/2 \rceil, \lceil j/2 \rceil}.$$

Each quadrant offset is estimated as the difference between its average pixel output $\overline{V}^q$ and the overall average pixel output $\overline{V}$, i.e., $\Delta_q = \overline{V}^q - \overline{V}$. The quadrant FPN variances $\sigma_{X^q}^2$ are estimated using a standard variance estimator.

Table V lists the estimated FPN results under dark conditions and at illuminations corresponding to 30% full well and 78% full well.

In our sensor, temporal noise is negligible compared to quantization noise. To see this, note that at 8 bits of resolution and assuming 2 V of signal swing, the standard deviation of quantization noise is around 2.3 mV. Our image sensor has a well capacity of around 90 000 e^-s. Even at the maximum signal value, the shot noise standard deviation is around 300 e^-. Using our sensitivity estimate of 5.1 μV/e^-, the 300 e^- correspond to 1.5 mV, which is significantly smaller than quantization noise. Noise from other sources such as k/TC, $1/f$ is much smaller than 300 e^-. Hence, quantization noise dominates. This conclusion is corroborated by measurements of our sensor.

VI. HIGH DYNAMIC RANGE VIA MULTIPLE SAMPLING

In this section, we describe how the image sensor implements multiple sampling, present a multiple sampling example, and discuss the limits on achievable dynamic range using multiple sampling.

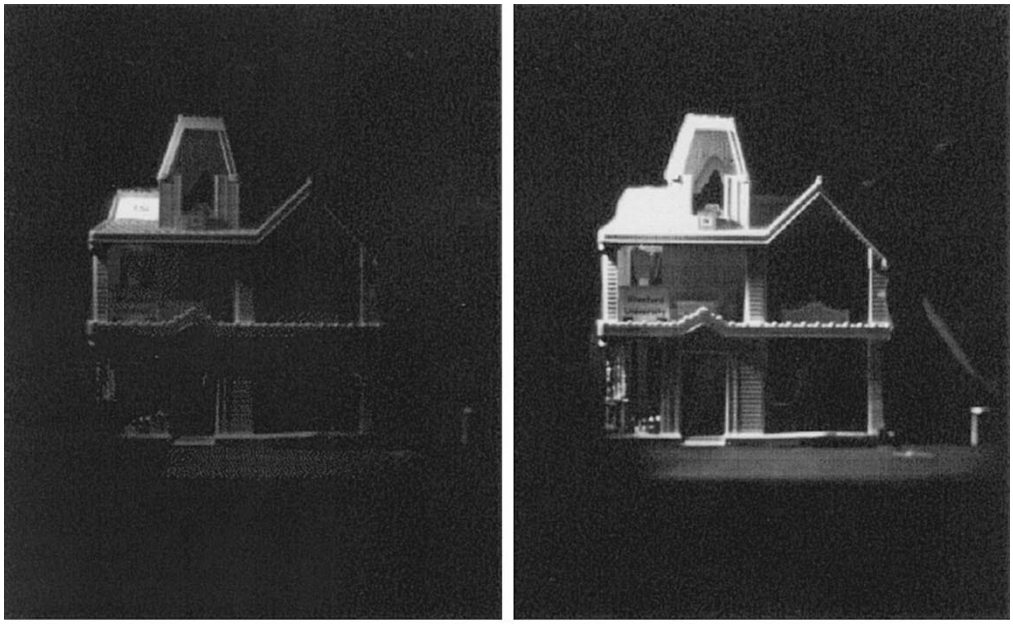
To perform multiple sampling, a scene is imaged one quarter frame at a time, as illustrated in Fig. 12. Before capturing a quarter frame, the sensor is reset. Sample and hold is used to ensure that the signal does not change during ADC. Each quarter sample image is read out one bit plane at a time [16]. The quarter images are then combined to form a quarter frame, and the quarter frames are merged into a high dynamic range frame.

A scene with measured dynamic range of more than 10^4 is illustrated in Figs. 17 and 18. The scene was sampled nine times, at $T = 3.3$ ms, $2T$, ..., and $256T$, and a 16-bit image was reconstructed. Since we cannot print grayscale images of more than 8 bits, we display four 8-bit slices of the image in Fig. 17. The first is a plot of the eight most significant bits of the 16-bit image, where only the roof and the front of the dollhouse are seen. The second was obtained by brightening the image by eight times. Several objects inside the house are revealed. These objects become more visible in the third image, after the original image was brightened by 32 times. The fourth image was obtained by brightening the image by 256 times. A table and a man hiding in the dark area next to the house appear. Fig. 18 is an 8-bit plot of the log of the 16-bit image. Note that all the objects can be seen in this image, albeit less clearly.

This example demonstrates that using multiple sampling, our sensor can achieve 16 bits of dynamic range, i.e., $2^{16}:1$. We now discuss the limits on achievable dynamic range.

First, it is important to distinguish between dynamic range, as the ratio of the sensor's largest nonsaturating signal to the standard deviation of the noise under dark conditions, and digital dynamic range, where the noise under dark conditions includes quantization noise and is therefore lower. Since the output of our sensor is digital, we focus on digital dynamic range. For our sensor, the standard deviation of the noise under dark conditions is much smaller than that of quantization noise, and therefore the digital dynamic range is simply $2^{k+m}:1$, where $m = 8$ is the maximum ADC resolution, and $k + 1$ is the number of samples. To achieve higher dynamic range, we need to increase k, i.e., sample as many times as possible.

(a) (b)



(c) (d)

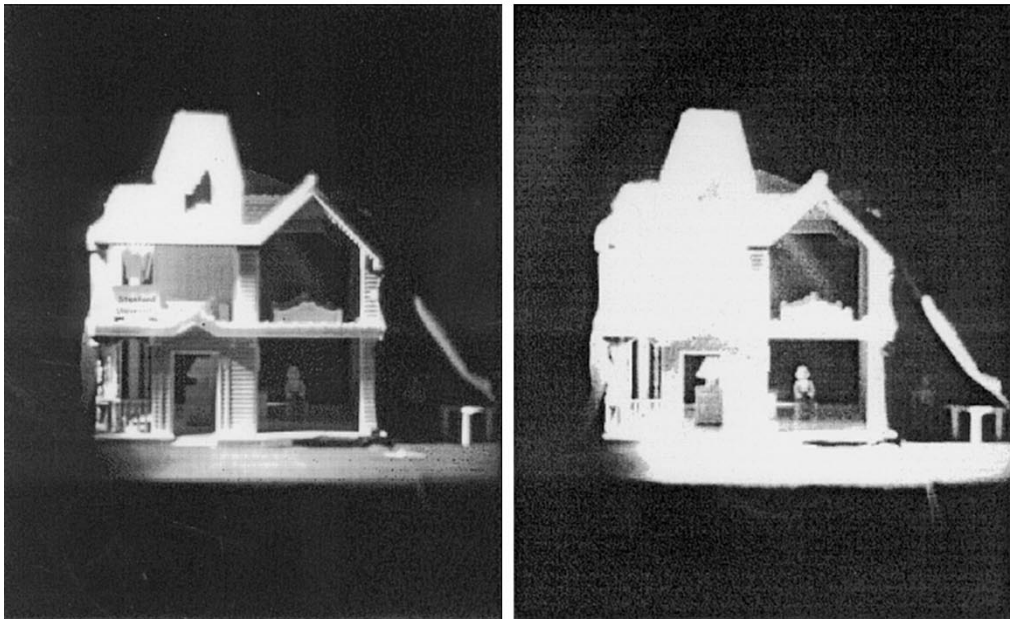


Fig. 17. Four slices of the 16-bit image. (a) Most significant 8-bit. (b) Image brightened eight times. (c) Image brightened 32 times. (d) Image brightened 256 times.

The maximum number of sampling times $k_{\max}$, however, is bounded by a lower bound on the shortest sampling time $T_{\min}$ and an upper bound on longest sampling time 2^kT, $T_{\max}$. The lower bound on $T_{\min}$ is dictated by the requirement that the m-bit conversion and the sensor readout for the first sample must be completed before the second sample. In [16], it is shown that the ADC requires $2^m - 1$ binary comparisons to complete a conversion; hence $T_{\min} \geq (2^m - 1)t_{\text{comp}} + t_r$ where t_{comp} is the comparison time, which depends on the comparator's gain-bandwidth product, and t_r is the readout time for m bits. In our implementation, $t_{\text{comp}} \approx 3.3$ μs for $m = 8$ bits, and the total readout time for 8 bits $t_r \approx 100$ μs, which yields $T_{\min} \approx 0.9375$ ms. The upper bound on the maximum sampling time $T_{\max}$ is set by the dark current. As exposure time increases, the fraction of the available signal voltage swing decreases by the accumulated dark charge. Since we require m bits of resolution from each sample, the decrease in available signal voltage swing must be less than 2^{-m} of the available voltage swing. Our total signal swing $V_{\max} \approx 2$ V. Therefore, for $m = 8$, we require that at $T_{\max}$, $V_{\text{dark}} < 7.8125$ mV. The dark signal D in mV/s is 1.31. Therefore, $T_{\max} = V_{\text{dark}}/D \approx 6$ s. Combining the two bounds, we get that $2^{k_{\max}} \leq 6400$, i.e., that the maximum digital dynamic range is $\approx 1.6 \times 10^6 : 1$.

The maximum sampling time $T_{\max}$ may also be limited by the user, e.g., for video applications. In this case, $2^{k_{\max}} = T_{\max}/T_{\min}$. For example, for 30-f/s operation, $T_{\max} = 33/4$ ms (the factor of four accounts for multiplexing),

Fig. 18. Eight-bit log of the 16-bit image.

$2^{K_{\max}} = 8.8$, and the digital dynamic range is 2 048 : 1, i.e., 11 bits.

Finally, dynamic range can be extended further by resetting to achieve lower $T_{\min}$. For example, to lower the minimum sampling time to $T_{\min}/2$, we reset the sensor after reading the first sample, then take the second sample after $T_{\min}$s, the third after $2T_{\min}$, and so on.

VII. Conclusion

We have shown that multiple sampling achieves consistently higher SNR at equal or better dynamic range than using well capacity adjusting. However, implementing multiple sampling requires readout speeds that are much higher than can be achieved by CMOS APS. We demonstrated using a 640 × 512 image sensor that pixel-level ADC enables a highly flexible and efficient implementation of multiple sampling to enhance dynamic range. Since pixel values are available to the ADC at all times and all ADC's operate simultaneously, the number and timing of the samples, as well as the number of bits for each sample, can be freely chosen and read out at fast SRAM speeds.

In particular, we demonstrated that by sampling a scene at exponentially increasing exposure times, very wide dynamic range pixel values with binary floating-point resolution can be obtained. Moreover, the ADC's in this case only need to output the minimum number of bits required to synthesize the high dynamic range image. We presented new modeling and characterization techniques especially suited for image sensors with Nyquist-rate pixel-level ADC. Using these techniques, we measured the image sensor QE, sensitivity, ADC transfer curve, and FPN. The results show that the sensor response is quite linear, which greatly simplifies the synthesis of high dynamic range images from multiple samples. The sensor also has very low ADC FPN due to autozeroing and the

sharing of the main ADC control signals. In conclusion, this paper demonstrates yet another important advantage of the use of pixel-level ADC—the ability to programmably enhance dynamic range with no loss in SNR.

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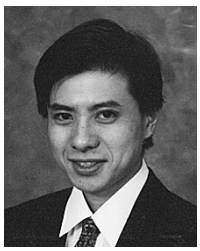

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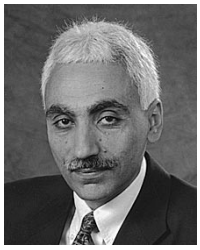
Dr. Yang was supported by a fellowship from Hewlett Packard Labs for two years and was a recipient of the 1998 Intel Foundation Fellowship.



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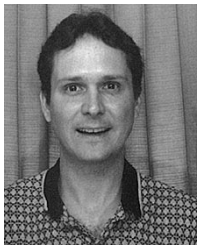

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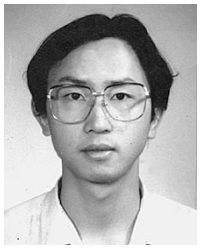
From 1995 to 1998, he worked at Stanford University as a Research Associate and helped to start the CMOS Image Sensor Center there. Presently he is working at Pixel Devices International, Sunnyvale, CA, where he is responsible for research and development of image sensors. He is the author or coauthor of more than 15 publications and five patents. His interests include CMOS image sensors, low noise analog electronics, image processing, and data compression.



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