Digital Pixel Image Sensors

Abbas El Gamal

Department of Electrical Engineering

Stanford University
Outline

- Background
- Programmable Digital Camera project
- Digital Pixel Sensor (DPS)
- Applications to Still and Video Imaging:
  - Dynamic Range Extension
  - Read noise reduction
  - Image blur prevention
- Experimental imaging system
- Conclusion
Background

- Digital cameras using CCD image sensors are rapidly replacing film and analog cameras
- CMOS image sensors are emerging as alternative to CCDs:
  - low fabrication cost
  - low power consumption
  - high frame rate non-destructive readout
  - camera-on-chip integration
- Enabling new imaging applications:
  - PC, web camera
  - cell phones and PDAs
  - toys and games
  - biometrics
  - camera arrays and networks
Digital Camera Implementations

Current implementations

Future

Functional block diagram

- Image Sensor
- ADC
- Color Processing
- Image Enhancement & Image Compression
- Control & Interface

- CCD
- Analog Proc & ADC
- Memory
- ASIC

- CMOS Image Sensor & ADC
- ASIC
- Memory

Single chip digital camera (camera-on-chip)
Image Sensors

- Image sensor consists of:
  - 2-D array of pixels, each containing a photodetector and devices for readout
  - circuits at periphery for amplification and readout
- Sensor size ranges from 320×240 (QVGA) for low end PC digital camera to 7000×9000 for scientific/astronomy applications
- Pixel size ranges from 15×15 μm or more down to to 4×4 μm
Collected charge is *simultaneously* transferred to the vertical CCDs at the end of integration time and then shifted out via horizontal CCD.

Charge transfer to vertical CCDs simultaneously *resets* the photodiodes – electronic shutter.
CCD Image Sensors

• Advantage: High quality
  – optimized photodetectors (high QE, low dark current)
  – low noise and nonuniformity (CCDs do not introduce noise or nonuniformity)

• Disadvantages:
  – inability to integrate other camera functions on same chip with image sensor
  – high power (due to high speed shifting clocks)
  – limited frame rate (due to analog serial readout)
Analog CMOS Image Sensors

- Pixel charge/voltage transferred one row at a time to column capacitors, then read out using column decoder/multiplexer
- Row integration times *staggered* by row readout time
Analog CMOS Image Sensor Pixel Architectures

- Passive pixel (PPS)
  - 1 transistor per pixel
  - small pixel, large fill factor, but
  - slow, low SNR

- Active pixel
  - 3-4 transistors per pixel (APS)
  - fast, higher SNR, but
  - larger pixel, lower fill factor

- As technology scaled to $0.5\mu m$ pixel size/fill factor
  not a problem – current technology of choice
Analog CMOS Image Sensors

- **Advantages:**
  - low power consumption
  - high frame rates
  - integration

- **Disadvantages:**
  - high noise and nonuniformity due to multiple levels of amplification (pixel, column, and chip)
  - sensitivity to digital noise coupling
  - analog circuits performance deteriorates in deep submicron CMOS
• Industrially funded research project by several companies including Canon, Agilent, HP, Kodak

• Objective: To develop and implement algorithms, architectures, and circuits for single chip programmable CMOS digital imaging systems
  – to achieve CCD/film quality (or better)
  – to enable new applications of digital imaging

• Program directed jointly with Prof. Brian Wandell (psychology)

• 12 PhD students have been supported under the program
PDC Program Main Accomplishments

• Developed the Digital Pixel Sensor architecture – A/D conversion performed at the pixel level (digital data directly read out of the pixel)

• Prototyped and successfully demonstrated 5 complete DPS chips, including world’s first 0.35μ and 0.18μ CMOS image sensors

• Demonstrated 10,000 frames/s (1Gpixels/s) operation using our most recent DPS chip

• Built a complete hardware/software environment for the DPS chips to explore several novel imaging applications

• Developed methods for analyzing and characterizing image sensor performance parameters (for PPS, APS, and DPS)
PDC Program Main Accomplishments – contd.

- Developed algorithms to exploit the high speed potential of DPS for high dynamic range, optical flow estimation, and motion blur prevention
- Developed a camera simulator (from object to color images), used it in several image sensor studies
- Developed a course on image sensors and digital cameras – lecture notes available via the class webpage
- Presented and published many papers (available through our webpages: http://www-isl.stanford.edu/abbas/group and http://smartcamera.stanford.edu/pdc.html)
- 5 PhDs completed, several nearing completion
Digital Pixel Sensor (DPS)

- ADC per pixel and all ADCs operate in parallel
- Advantages:
  - high speed digital readout
  - no column read noise or Fixed Pattern Noise
  - scales well with CMOS technology
Block Diagram of Digital Pixel Sensor
Transistors Per Pixel as Technology Scales

- DPS Problem: large pixel size
- As technology scales, pixel size approaches limit set by optics and dynamic range constraints
- Assuming a 5\(\mu\)m pixel at 30% fill factor:

<table>
<thead>
<tr>
<th>Year</th>
<th>Digital</th>
<th>Analog</th>
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<tbody>
<tr>
<td>1995</td>
<td>0.35</td>
<td>0.01</td>
</tr>
<tr>
<td>1997</td>
<td>0.25</td>
<td>0.02</td>
</tr>
<tr>
<td>1999</td>
<td>0.18</td>
<td>0.03</td>
</tr>
<tr>
<td>2000</td>
<td>0.15</td>
<td>0.04</td>
</tr>
<tr>
<td>2001</td>
<td>0.13</td>
<td>0.05</td>
</tr>
<tr>
<td>2003</td>
<td>0.10</td>
<td>0.06</td>
</tr>
<tr>
<td>2006</td>
<td>0.07</td>
<td>0.07</td>
</tr>
<tr>
<td>2012</td>
<td>0.05</td>
<td>0.08</td>
</tr>
</tbody>
</table>

![Graph showing the number of transistors per pixel over time]
Pixel-level ADC Architectures

- First order sigma delta modulation (ISSCC’94)
- Multi-channel Bit-Serial ADC (JSSC’99)
- Single-slope bit-parallel ADC (JSSC’01)
MCBS ADC highlights

- Nyquist rate bit serial ADC
- Requires only 1-bit comparator and 1-bit latch per pixel or per group of neighboring pixels – very simple circuits
- Control signals shared by all ADCs – low pixel FPN
- Supports programmable step size quantization
- Implementation supports autozeroing and electrical testability of all circuits (except photodiodes)
How 1-bit Comparator/Latch Works
640 × 512 DPS Chip Characteristics (Yang ISSCC’99)

- 0.35µm CMOS technology
- 640 × 480 pixels (VGA)
- 10.5µ × 10.5µ pixels
- 22 transistors per 2×2 pixel block
- 1 million transistors
- 8 bit MCBS pixel level ADC
- 32 wide digital output bus
- < 100 frames/s
High Speed DPS Chip Goals

- Demonstrate high speed advantage of DPS
  - first imager to achieve 10,000 frames/s and 1 Gpixels/s continuous imaging

- Demonstrate the scaling advantage of DPS
  - first imager built in state of the art (0.18μm) CMOS technology

- Demonstrate DPS with bit-parallel ADC and pixel level digital memory
  - earlier implementations (Fowler ‘94, Yang ‘99) employed bit-serial ADCs

- Explore applications of high speed imaging to digital still and video imaging
DPS Chip Characteristics (Kleinfelder ISSCC‘01)

- 0.18μm CMOS technology
- 352 × 288 pixels (CIF)
- 9.4μ × 9.4μ pixels
- 37 transistors/pixel
- 3.8 million transistors
- 8 bit single slope ADC and memory/ pixel
- 64 wide digital output bus at 167 MHz
ADC Operation

Counter
(Gray Code)

Ramp
Input

Comp. Out
Digital Out

Memory Loading
Memory Latched

Latched Value

Gray Code Counter

Ramp
Input

Comp. Out
Digital Out
Still Image at 1,000 FPS
Video Sequence at 10,000 FPS

Frame 1

Frame 11

Frame 21

Frame 31
High Frame Rate Enables New Applications

- High frame rate enables new still and video imaging applications:
  - Dynamic range extension
  - Motion blur prevention
  - Motion estimation
  - Video compression
  - Video stabilization
  - Feature tracking
  - Super-resolution

- Integration of capture and processing on same chip enables low cost implementation of such applications
Basic Idea – Multiple-Capture Single-Image

- Operate the image sensor at high frame rate
- Process high frame rate data on-chip
- Output still or video images with any application specific data at standard frame rate
High Dynamic Range Imaging Problem

- Some scenes contain very wide range of illumination with intensities varying over 100 dB range or more
- Biological vision systems and silver halide film can image such high dynamic range scenes with little loss of contrast information
- Dynamic range of solid-state image sensors varies over wide range:
  
  - high end CCDs: $> 78$ dB
  - consumer grade CCDs: 66 dB
  - consumer grade CMOS imagers: 54 dB

- So, except for high end CCDs, image sensor dynamic range is not high enough to capture high dynamic range scenes
Example

HDR Scene

Short Exposure-time Image  Medium Exposure-time Image  Long Exposure-time Image
Extending Dynamic Range via Multiple Capture

- Sensor dynamic range is the ratio of:
  - highest nonsaturating signal – limited by well capacity, to
  - smallest detectable signal – limited by read noise

- Short exposure time increases highest signal

- Long exposure time reduces smallest signal

- In scene with high lights and dark shadows, need spatially varying exposure time

- Idea: Capture several images with different exposure times – combine them into high dynamic range image
  - need high speed readout
Multiple Capture Example
HDR Image Synthesis

Last-Sample-Before-Saturation (LSBS) Algorithm: For each pixel use an appropriately scaled version of its last sample before saturation
Limitation of LSBS Algorithm

- For a given maximum exposure time, it only enhances dynamic range at *high* illumination
  - Read noise is *not* reduced
- Increasing maximum exposure time limited by *motion blur*

![Input](image1.png)  ![Short exposure](image2.png)  ![Long exposure](image3.png)
Decreasing Read Noise (Liu SPIE’01)

- Estimate each pixel's signal using all its captured values (before saturation)
  - Weighted averaging reduces read noise – extends dynamic range and improves SNR at low illumination
- Developed a pixel-wise recursive estimation algorithm for reducing read noise
  - low computational complexity and small memory
  - well suited to camera-on-chip implementation
Optimal Weights

Longer exposure time samples weighted higher than shorter exposure time samples

- 32 samples
- $i_{ph} = 5fA$
- $i_{dc} = 1fA$
- $\sigma_V = 60e^-$
Read Noise Reduction

![Graph showing Read Noise RMS (e-) vs. Number of Samples (k) with two lines representing 'Without estimation' and 'With estimation'.]
Dynamic Range and SNR Improvements

![Graph showing dynamic range and SNR improvements]

- Estimation & LSBS
- Single Capture

DR = 47 dB

DR = 85 dB
Image Blur Prevention (Liu ICASSP‘01)

- For each pixel:

```
Initial Estimate

Next sample

Saturation or Motion detected?

Yes → End

No → Update Estimate

End
```

- Method is pixel-wise and recursive
  - small memory, independent number of captures
  - low computational complexity
  - well suited to camera-on-chip implementation
Motion Blur Prevention Example

Initial position

Final position

Conventional sensor

Our Method
Blur Prevention Used to Increase Exposure Time

Input

Short exposure

Long exposure

Our Method
Optical Flow Estimation via Multiple Capture

- Optical flow examples:

- Applications:
  - Compression
  - 3D motion and structure estimation
  - Video stabilization
  - Tracking

- Accuracy is of primary concern
Simulation Results (Suk Hwan ICIP’01)

- Synthetic sequences (30 and 120 frames/s) are generated by image warping

- Average angular error results:

<table>
<thead>
<tr>
<th>Scene</th>
<th>LK at 30 frames/s</th>
<th>Our method at 120 frames/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.43°</td>
<td>3.43°</td>
</tr>
<tr>
<td>2</td>
<td>3.94°</td>
<td>2.91°</td>
</tr>
<tr>
<td>3</td>
<td>4.56°</td>
<td>2.67°</td>
</tr>
</tbody>
</table>

- Gain FPN correction (SukHwan SPIE’02)
Experimental High Speed Imaging System

- Built around our 10,000 frames/s DPS chip
- Interfaced to PC
- Programmable via Matlab interface
65 Image Capture Example

0ms

10ms

20ms

30ms

40ms

50ms
High Dynamic Range Image Synthesis

LSBS

Estimation/ Motion Detection
Conclusion

- Described Digital Pixel Sensor architecture and example implementations
- Presented applications of high speed imaging to still and video rate imaging
- Showed results that demonstrate the effective implementation of these applications using DPS
- Example of interdisciplinary research (circuit design, imaging, signal and video processing)
- Current research: Explore new applications of CMOS image sensors to:
  - biology
  - 3D imaging
  - biometrics