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Pixel Level Processing — Why, What, and How?
Background

- pixel level
- column level
- chip level

• Processing can be integrated at:

  - Processing

  - Require very significant analog and digital
digital cameras and computational sensors, which
  "Important for emerging imaging systems, e.g."

• Cost
cost

• Sensing and processing — lower system power and

• CMOS technology enables the integration of image
this research

Small pixel limits the commercial application of

results (CIGC98, ISSCC99)

Recent work on pixel level ADC – promising

computational sensors (Tanner84, Ayrer95, 96)

Significant work on analog pixel processing

Very active research on pixel level processing

pixel level used only for signal conditioning

column level processing (Langen98, Smith98)

Today’s CMOS digital cameras employ chip and

Background cont'd.
More programmable

- Higher performance imaging

- Processors prefered over analog pixel processing

Pixel level ADC + pixel/column/chip level digital

- Transistors can be integrated at pixel level

- Considerations as to technology scales more

- Pixel size limited by optical and performance

- It promises very significant advantages

- Popular as technology scales

Pixel level processing will become increasingly

Thesis
Future directions

- Implementation and Results
- Operation of our MCBS ADC
- Why pixel level ADC

Pixel level ADC

Analog pixel processing

Historical perspective

Why pixel level processing?
Pixel size is the main constraint!

Dynamic range (15SSC98,99

Processing during integration: e.g., programmable

to ADC, very low BW needed

chip/column approaches (Rousumgur) – signals close

High SNR: Pixel level ADC offers higher SNR than

power supply voltages

operate the digital processors at very low

use subthreshold analog circuits, or

use very low speed processors

Low power: Parallel processing makes it possible to

Why Pixel Level Processing
and SNR
relative dark current increase limit
dynamic range

Performance limit – well capacity decrease and

size due to diffraction limit

Optics limit – cost increases with decrease in pixel

Pixel size limited to $\frac{\lambda}{4f}$ on side

Limit of Pixel Size
Assuming 5um pixels at 30% fill factor

Transistors per Pixel as Technology Scales

Technologies (μm)

Year


0.35 0.25 0.18 0.15 0.13 0.10 0.07 0.05

Analog
Digital

Transistors

312 66 128 256 54 32 16 8 4 2 1

W= D
As technology scaled to 0.5\(\mu\)m pixel size/3x factor, not a problem – current technology of choice

- Larger pixel, lower 3x factor
- Fast, higher SNR, but
- 3-4 transistors per pixel
- Active pixel (mid 90s –)

- Slow, low SNR
- Small pixel, large 3x factor, but
- 1 transistor per pixel
- Passive pixel (late 80s – early 90s)

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CMOS Image Sensor Evolution – From PPS to APS
Evolution of PPS and APS pixel sizes
Future directions •

Implementation and Results

Operation of our MCBS ADC

Why pixel level ADC

Pixel Level ADC

Analog pixel processing

Historical perspective

Why pixel level processing?
artificial retina (Astrom96, Brajovic96, Palei978) globally on groups of pixels – computational sensors, the pixel signals – signal conditioning, dynamic range.

We classify the work into:

Analog Pixel Processing

Inter-pixel processing performed locally or

(Dickson95)

Enhancement (Mead85, Decker98), compression
Dynamic range enhancement (Decker 98)

CDS and frame differencing (Dicke 95, Mendis 97)

Signal amplification

Electronic shuttering

Anti-blooming

APS transistors also used for

Analog Intrapixel Processing
Not programmable – chips are application specific

At lower resolution

However

power than using digital
implemented with fewer transistors and at lower

Using analog circuits more functionality can be

Why

Inter-Pixel Analog Processing
Outline

- Future directions
- Implementation and Results
- Operation of our MCBS ADC
- Why pixel level ADC
- Pixel level ADC
- Analog pixel processing
- Historical perspective
- Why pixel level processing?
Column Level

Chip Level

Approaches to ADC Integration
- Very limited silicon area
- But
- CMOS
- Process portability – compatible with digital
- Scalable sensor architecture
- Lowest power
- Highest SNR
- ADC close to signal generation always better

Pixel level ADC
simple and robust circuits are a must

ADCs, e.g., SA, algorithmic

Cannot use conventional Nyquist rate bit-serial

— bit-serial is more appropriate

down to 0.25µm

Cannot use bit-parallel ADCs for technologies

Constraints of Pixel Level ADC
High output data rate - need decimation
Moderate fixed pattern noise
Poor low light response
Pixel size too large - 20 mm in 0.8 mm technology

Limitations:
Simple inexpensive circuits can be used
Pixels operate simultaneously
1-bit first order ∇ADC per pixel or per four

Pixel Level Sigma Delta ADC (ISSCC94, CICC96)
• Provides in-pixel testability
• Provides programmable step size quantization
• Lowers fixed pattern noise
• Improves low light response
• Reduces output data rate

Multi-channel bit-serial (MCBS) ADC
ADC Implements a Quantization Table

**Key Point:** Each output bit is a function of signal – can be separately generated.

<table>
<thead>
<tr>
<th>Gray Code</th>
<th>ADC Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 1</td>
<td>0</td>
</tr>
<tr>
<td>1 0 1</td>
<td>8</td>
</tr>
<tr>
<td>1 1 1</td>
<td>8</td>
</tr>
<tr>
<td>1 1 0</td>
<td>8</td>
</tr>
<tr>
<td>0 1 0</td>
<td>8</td>
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<tr>
<td>0 1 0</td>
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</tr>
<tr>
<td>1 0 0</td>
<td>8</td>
</tr>
<tr>
<td>0 0 0</td>
<td>8</td>
</tr>
</tbody>
</table>

ADC Method
3-bit Flash ADC (Not MICES ADC)
How 1-bit Comparator/Latch Works
Block Diagram for Image Sensor with Pixel Level ADC
Output of Image Sensor with Pixel Level ADC
<table>
<thead>
<tr>
<th>Maximum Frame Rate</th>
<th>ADC Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>250 frames/s (≈ 8-bit resolution)</td>
<td>8 bit</td>
</tr>
<tr>
<td>8 bit</td>
<td>3.3V</td>
</tr>
<tr>
<td>180 pin PGA</td>
<td>Transistors per pixel</td>
</tr>
<tr>
<td>5.9 (22 per four pixels)</td>
<td>Ffill Factor</td>
</tr>
<tr>
<td>29%</td>
<td>Sensor area</td>
</tr>
<tr>
<td>6720 µm × 5376 µm</td>
<td>Photodetector</td>
</tr>
<tr>
<td>n-well/p-sub diode</td>
<td>Pixel size</td>
</tr>
<tr>
<td>10.5 µm × 10.5 µm</td>
<td>Sensor size</td>
</tr>
<tr>
<td>640 × 512 pixels</td>
<td>Technology</td>
</tr>
<tr>
<td>0.35 µm, 4-layer metal, 1-layer poly, n-well CMOS</td>
<td></td>
</tr>
</tbody>
</table>
Multiplexed MCBS ADC Pixel Block Circuit Schematic
Pixel Block Layout
Die micrograph of 640 × 512 Image Sensor
Pixel Array

640 x 512

Row Decoders

Sense Amps & Latches
Experimental Setup for Imager Characterization
Measured ADC Transfer Curve
- 8-bit resolution
- 29% Fill factor
- 10.5 × 10.5 μm

CMOS process
A 640 × 512 image in a 0.35 μm 4-metal layer

- Electrically testable
- Very low power
- Simple circuits
- First Nyquist rate pixel level ADC technique

MGBS ADC Summary
$$m \times n \times \text{readout}_\text{pixel} + \text{readout}_\text{chip} = \text{readout}_\text{pixel}$$

Sensor with pixel level ADC

$$n \times \text{ADC} + n \times \text{readout}_\text{chip} = \text{readout}_\text{chip}$$

APS with column level ADC

$$n^2 \times \text{ADC} + n^2 \times \text{readout}_\text{chip} = \text{readout}_\text{chip}$$

APS with chip level ADC

Resolution

Readout speeds for n x n pixel imager @ m-bit

Readout Speed - Real Advantage of Pixel Level ADC
15K frames/s for pixel ADC vs. 700 for column ADC.

\[ 25\mu s + 5\mu s = 8 \times 10^3 \times 10^3 \times 1.4\mu s = 4\mu s \times 1.4\mu s = 1.4\mu s \]

Sensor with pixel level ADC

\[ 400\mu s \times 1.4\mu s + 20\mu s \times 0.1\mu s = 120\mu s \]

APS with column level ADC

\[ 400\mu s \times 1.4\mu s = 560\mu s \]

APS with chip level ADC

Consider 1000 × 1000 imager @ 8-bit

Readout Speed Comparison
Military applications •
Industrial applications •
Motion estimation •
(ISSCC'99, 3649-28)
Enhance dynamic range via multiple sampling •

Applications of Fast Readout Speed
Future directions

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– Historical perspective
– Why pixel level processing?
Pixel Level ADC requires very simple and robust weak

perform more processing with less area/power weaker

– argument that analog circuits perform more processing in less area/power

– Digital circuits scale well argument that analog

scalable, increased device leakage

– Analog circuits scale poorly – power supply

mainstream

Interpixel analog processing is unlikely to become

processing

More transistors available at pixel level

Future of Pixel Level Processing
circuits

analog circuits, minimizes the need for analog
Assuming 30% Fill Factor

Estimated Pixel Size of MCMs ADC
Assuming 5μm pixel, 30% fill factor, non-multiplexed

Number of DRAM and SRAM Bits in a Pixel

MICBS ADC
a-si, pixel area is free for adding memory and processing

If photodeector is moved to top of silicon, e.g. using

• Lower power consumption
• Frame storage
• Pipelining for faster readout
• Store local state information

Why Pixel Level Digital Memory
during integration

Especially for applications requiring processing
implementing programmable computational sensors

• Significant advantages to image capture and for

Interpixel Digital Processing
Processing

borrow from vast literature on the grain paradigm

Architecture and programming paradigm can

and different computational sensor applications

Programmable for different imaging environments

Programmable Pixel Sensors