Analysis of Temporal Noise in CMOS APS

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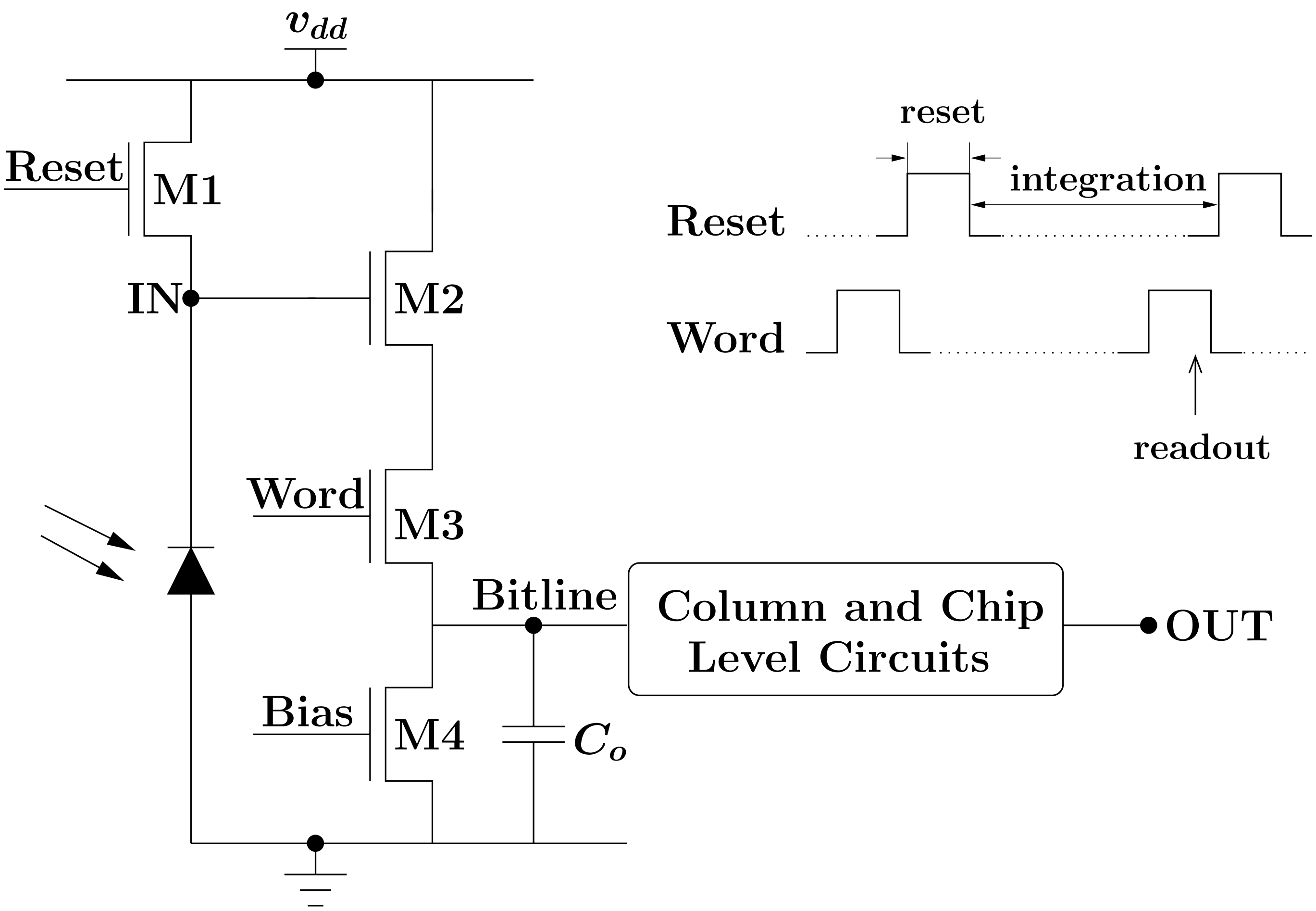
Motivation

- **Temporal noise limits image sensor performance**
- **CMOS APS has more noise sources than CCD does**
  - **Pixel reset transistor**
  - **Readout circuits**
- **Previous noise analysis (Yadid-Pecht SPIE97, Mendis JSSC97, Decker JSSC98)**
  - **Assume that sensor response is linear**
  - **Assume steady state is achieved during reset to get $\frac{kT}{C}$**
- **Experiments showed observable nonlinearity and that reset noise is substantially smaller than $\frac{kT}{C}$**

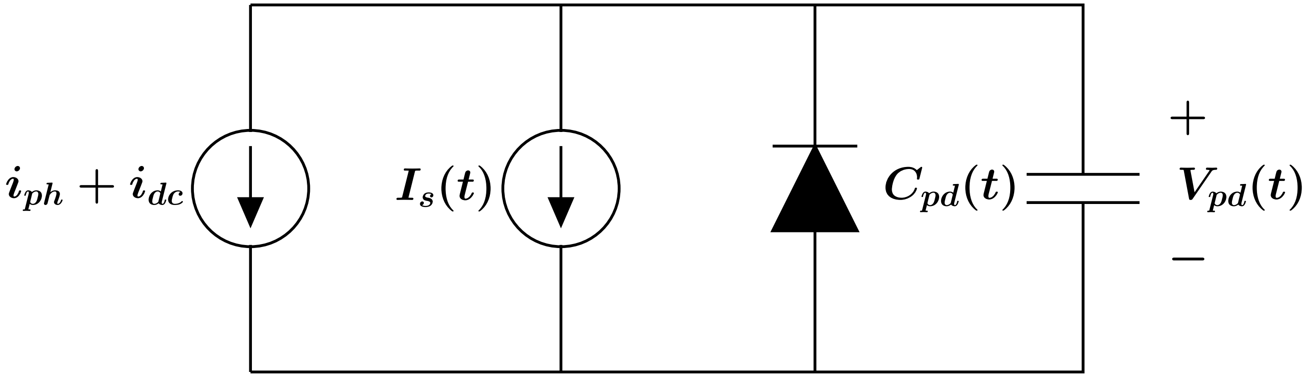
APS Circuit and Operation



Outline

- **Noise during integration**
- **Noise during reset**
- **Noise during readout**
- **Experimental results**
- **Conclusion**

Noise During Integration: Model



- Shot noise $I_s(t)$ dominates, with psd

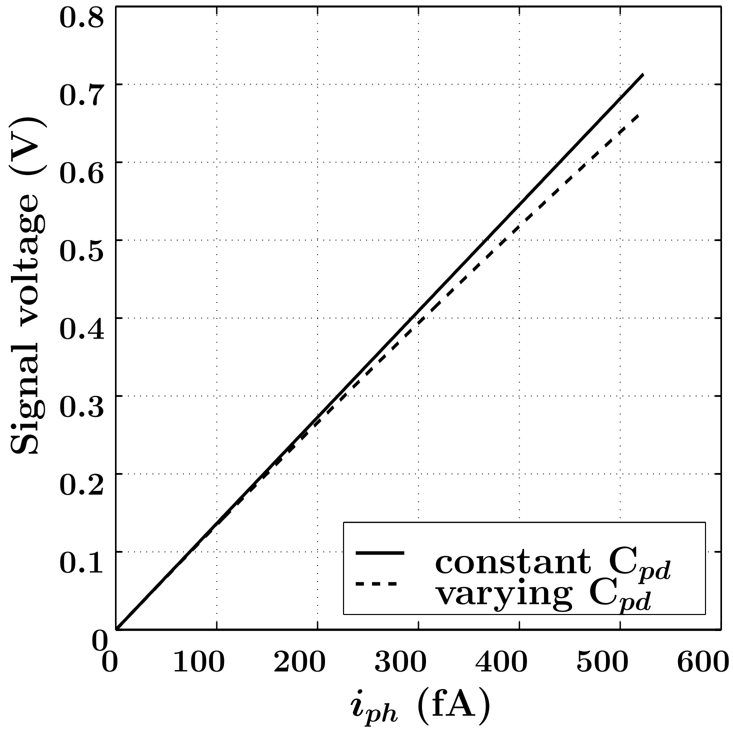
$$S_{I_s}(f) = q(i_{ph} + i_{dc}) \ \ \mathrm{A}^2/\mathrm{Hz}$$

- Circuit equation

$$\frac{dV_{pd}(t)}{dt} = -\frac{i_{ph} + i_{dc} + I_s(t)}{C_{pd}(V_{pd}(t))}$$

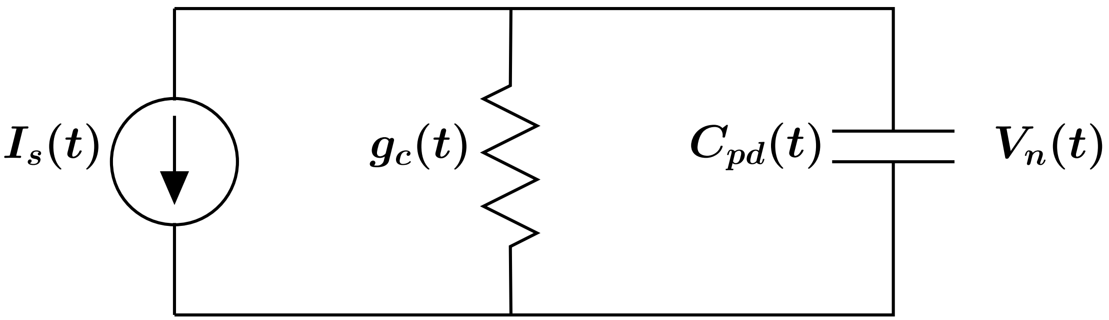
Deterministic (Signal) Part

- **First analyze the deterministic part to get $v_{pd}(t)$, $C_{pd}(v_{pd}(t))$, and $\frac{dC_{pd}(v_{pd}(t))}{dv_{pd}(t)}$**
- **Assume abrupt** pn **junction in varying C_{pd} case**



Noise Part

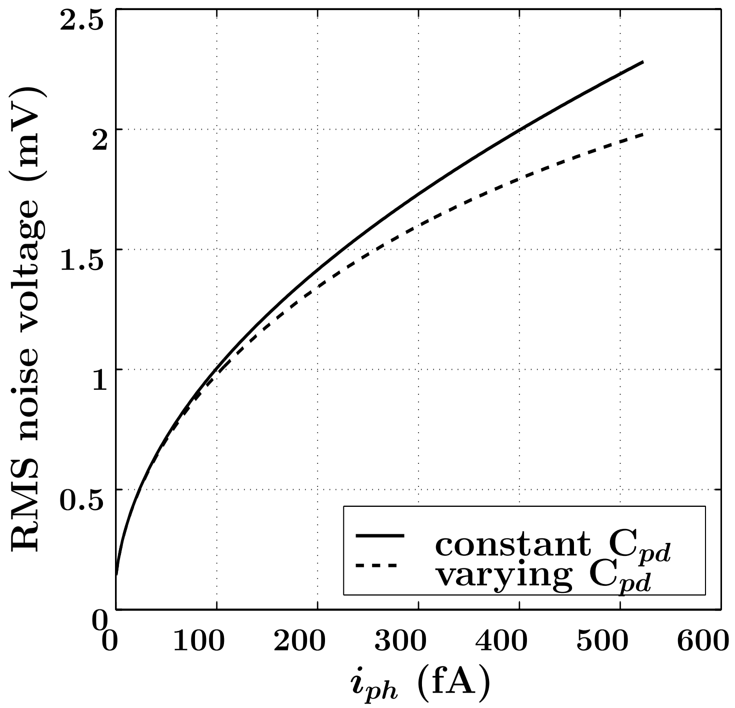
- **Analyze the noise part with equivalent small signal model**



$g_c(t) = -\frac{(i_{ph}+i_{dc})}{C_{pd}(v_{pd}(t))}\frac{dC_{pd}(v_{pd}(t))}{dv_{pd}(t)}$ **is the nonlinearity induced conductance**

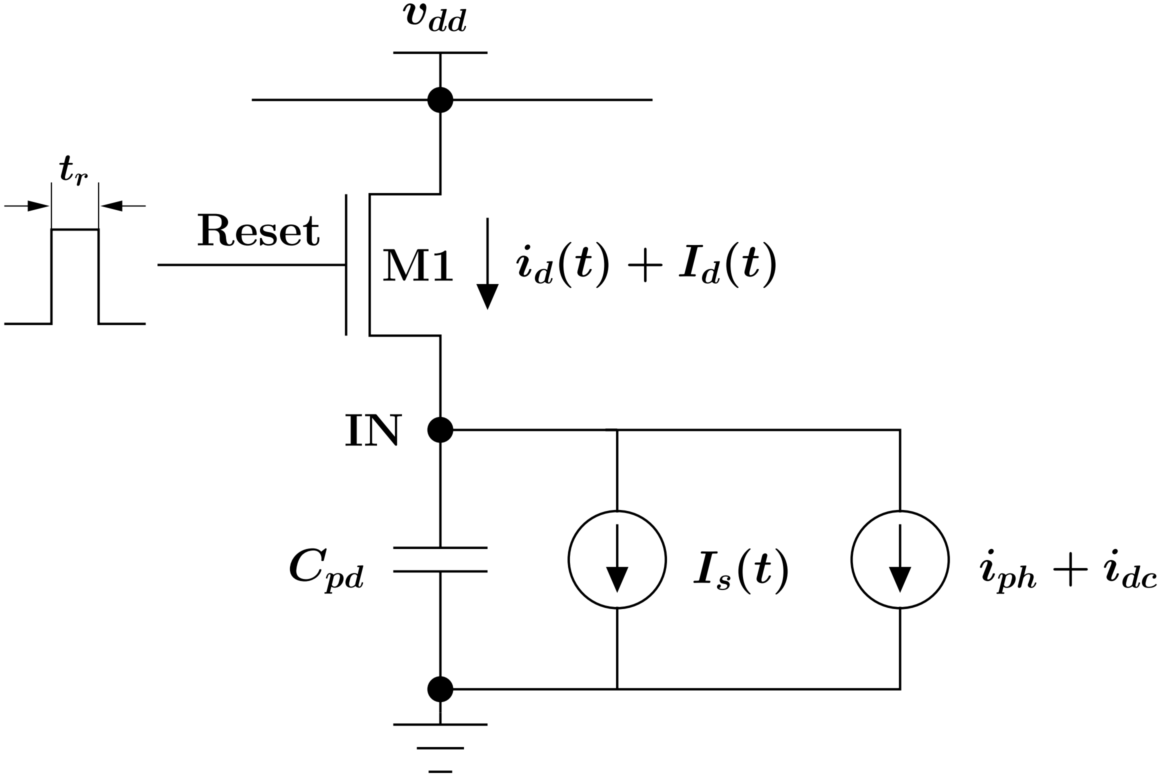
Noise During Integration: Results

- Still assume abrupt *pn* junction



- Technology scaling and some SNR expansion schemes lead to more pronounced nonlinearity

Noise During Reset: Model

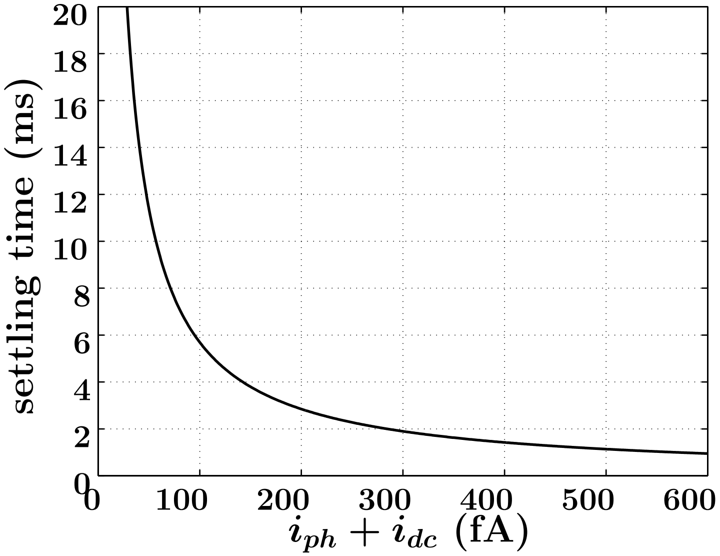


- **Subthreshold shot noise $I_d(t)$ has psd**

$$S_{I_d}(f) = q i_d(t) \ \ \mathrm{A}^2/\mathrm{Hz}$$

Settling Time

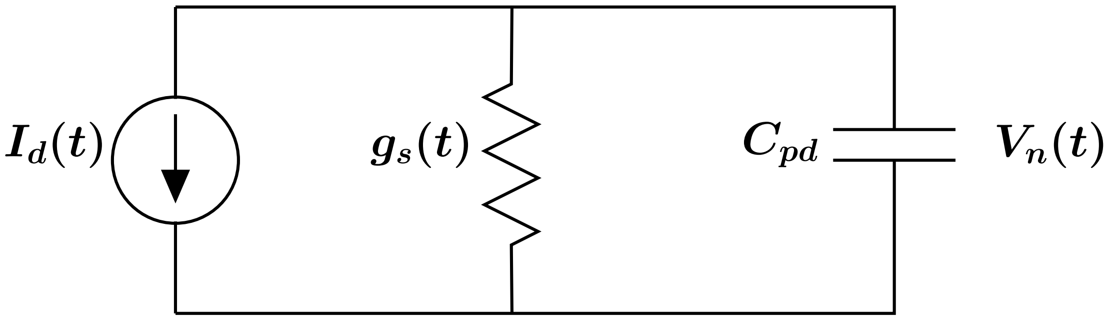
- In steady state, it is well known that $\overline{V_n^2} = \frac{kT}{C_{pd}}$
- But to attain steady state, IN voltage must be constant, which happens only when $i_d = i_{ph} + i_{dc}$



- Need > 1ms to achieve steady state, while t_r is few μs. So Steady state is not attained during reset.

Noise Model

- Use small signal model as before



$g_s(t) = \frac{q i_d(t)}{kT}$ is subthreshold transconductance

$$i_d(t) = \frac{W}{L} I_0 e^{\left[\frac{(v_g - v_{pd})\kappa}{v_T} - \frac{(v_{pd} - v_b)(1-\kappa)}{v_T}\right]} (1 - e^{\frac{(v_d - v_{pd})}{v_T}})$$

- Solution to this general linear time varying system

$$\overline{V_n^2(t_r)} = \int_0^{t_r} \frac{N(\tau)}{C_{pd}^2(\tau)} e^{-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}(\tau_0)} d\tau_0} d\tau$$

Noise During Reset: Results

- Surprisingly easy to evaluate, and the final result of noise is neat

$$\overline{V_n^2(t_r)} = \frac{1}{2}\frac{kT}{C_{pd}}\left(1 - \frac{\delta^2}{(t_r - t_1 + \delta)^2}\right)$$

  - Transition time $t_1 \leq 0.2$ns
  - Thermal time $\delta \equiv \frac{v_T C_{pd}}{i_d(t_1)} \approx 6$ns

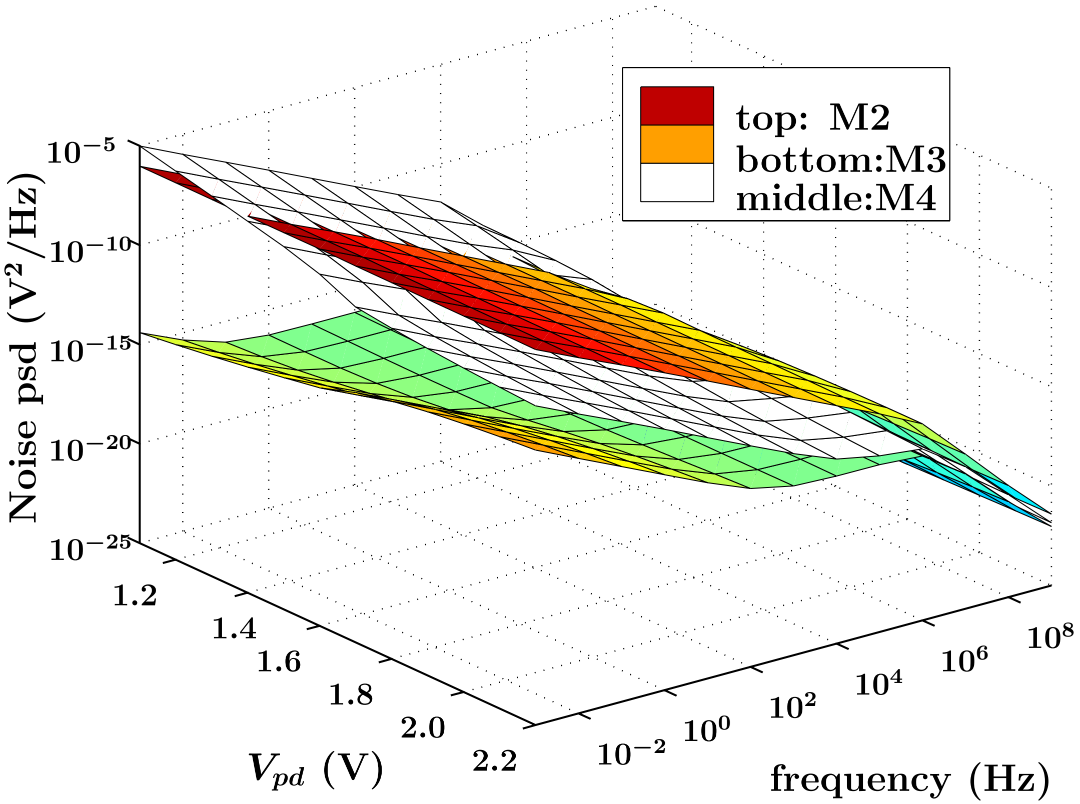
- Only half of the commonly quoted $\frac{kT}{C_{pd}}$!!
- Output referred RMS noise voltage is 245 μV

Noise During Readout

- **Analysis done using HSPICE simulation (both thermal and 1/f noise)**
  - **Sweep IN voltage to get the DC point**
  - **Perform AC noise analysis at each point**
- **Results**
  - **Noise from column and chip level circuit is negligible**
  - **Noise from access transistor is much lower than noise from follower or bias transistor**
  - **Output referred RMS noise voltage is 63μV**

Noise Contributed by different Transistors

- **Readout noise psd due to M2, M3, and M4, at different signal voltages**



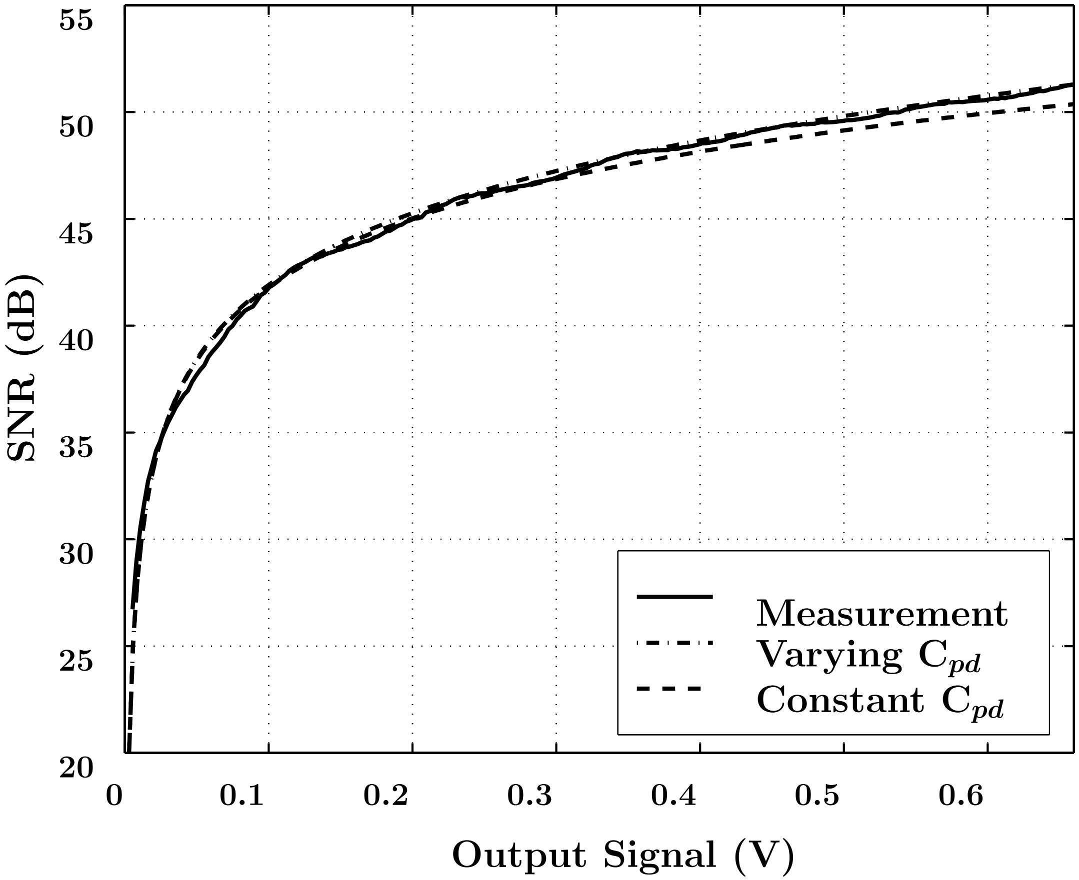
Experiments

- **Use 64×64 pixel APS test structure (AFPAEC96)**
- **Same optical and electrical setup used for QE and FPN measurements (SPIE98)**
- **Special care taken to reduce environmental interference**
- **Measured board level RMS noise voltage is 82μV**

Reset Noise Experiments

- **Reset is followed immediately by readout**
- **Reset time varied from 1μs to 10μs**
- **Experiments done at several illumination levels**
- **Measured RMS noise voltage $\approx$ 285μV vs. 253μV from analysis (lower than 353μV from $\frac{kT}{C}$ estimate)**

SNR vs. Output Signal Voltage



Conclusion

Accurate analysis of temporal noise in photodiode APS

- **Noise during reset**
  - **Noise is half the commonly quoted $\frac{kT}{C}$ value**
- **Noise during integration**
  - **Nonlinearity improves SNR at high illumination**
- **Noise during readout**
  - **Follower and bias transistor contribute most of the noise**

Experimental results corroborate analysis results