Characterization of CMOS Image Sensors with Nyquist Rate Pixel Level ADC

David Yang, Hui Tian, Boyd Fowler, Xinqiao Liu, and Abbas El Gamal

Information Systems Laboratory, Stanford University, Stanford, CA

Motivation

- **Characterization techniques for CCDs modified and extended for CMOS APS, PPS (Janesick'87, Fowler'98, ElGamal'98)**
- **Pixel level ADC imagers require further modification**
  - **No analog output**
  - **Limited output resolution (e.g. 8-bit)**
- **Develop characterization techniques for pixel level ADC imagers**

Outline

- **Pixel Level ADC Operation**
- QE, Sensitivity, and ADC Transfer Curve
- FPN

640×512 Image Sensor Characteristics

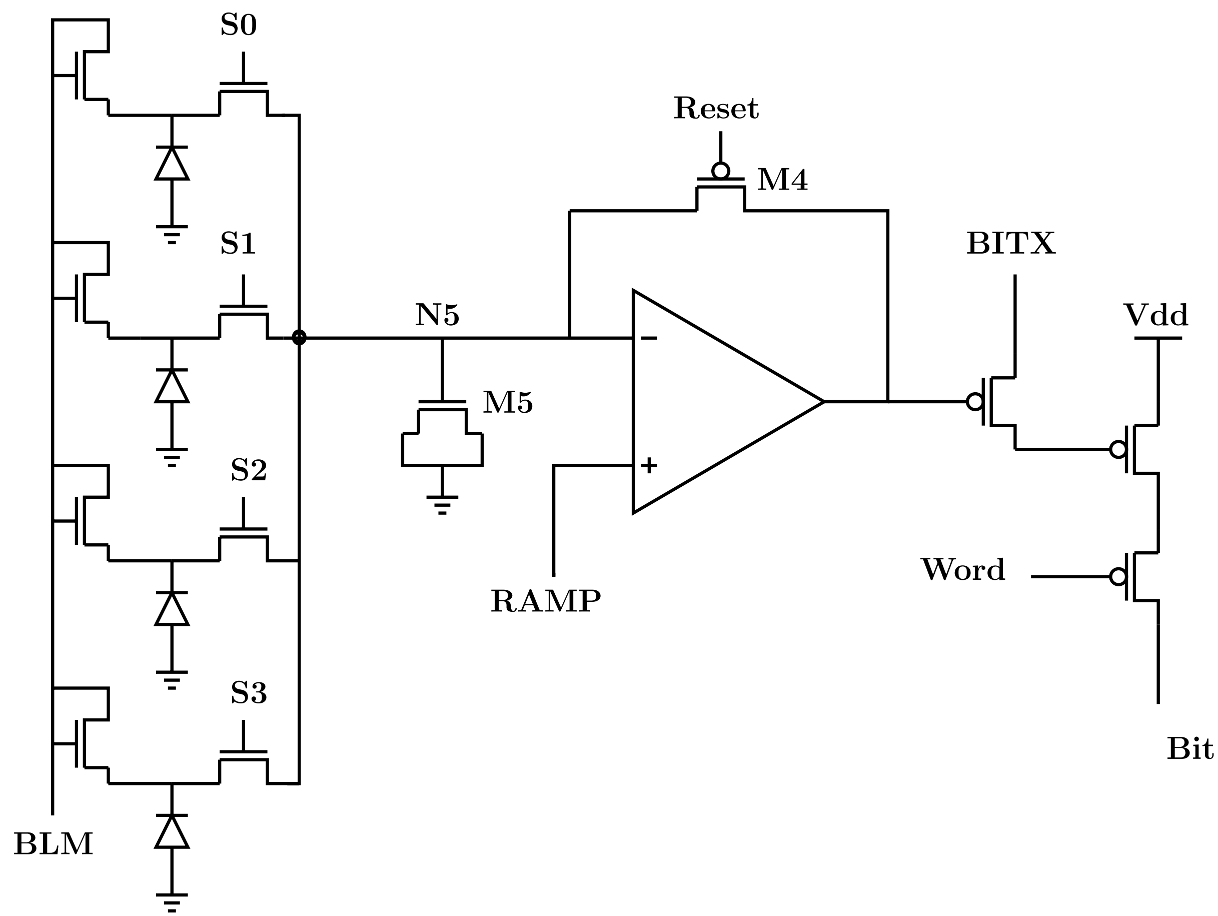
Technology	**0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS**
Sensor size	**640 × 512 pixels**
Pixel size	**10.5 μm × 10.5 μm**
Photodetector	**n-well/p-sub diode**
Sensor area	**6720 μm × 5376 μm**
Fill factor	**29%**
Transistors per pixel	**5.5 (22 per four pixels)**
Package	**180 pin PGA**
Supply voltage	**3.3V**
ADC resolution	**8 bit**
Maximum frame rate	**250 frames/s (@ 8-bit resolution)**

Pixel Level ADC Operation

Multi-channel Bit Serial (MCBS) ADC

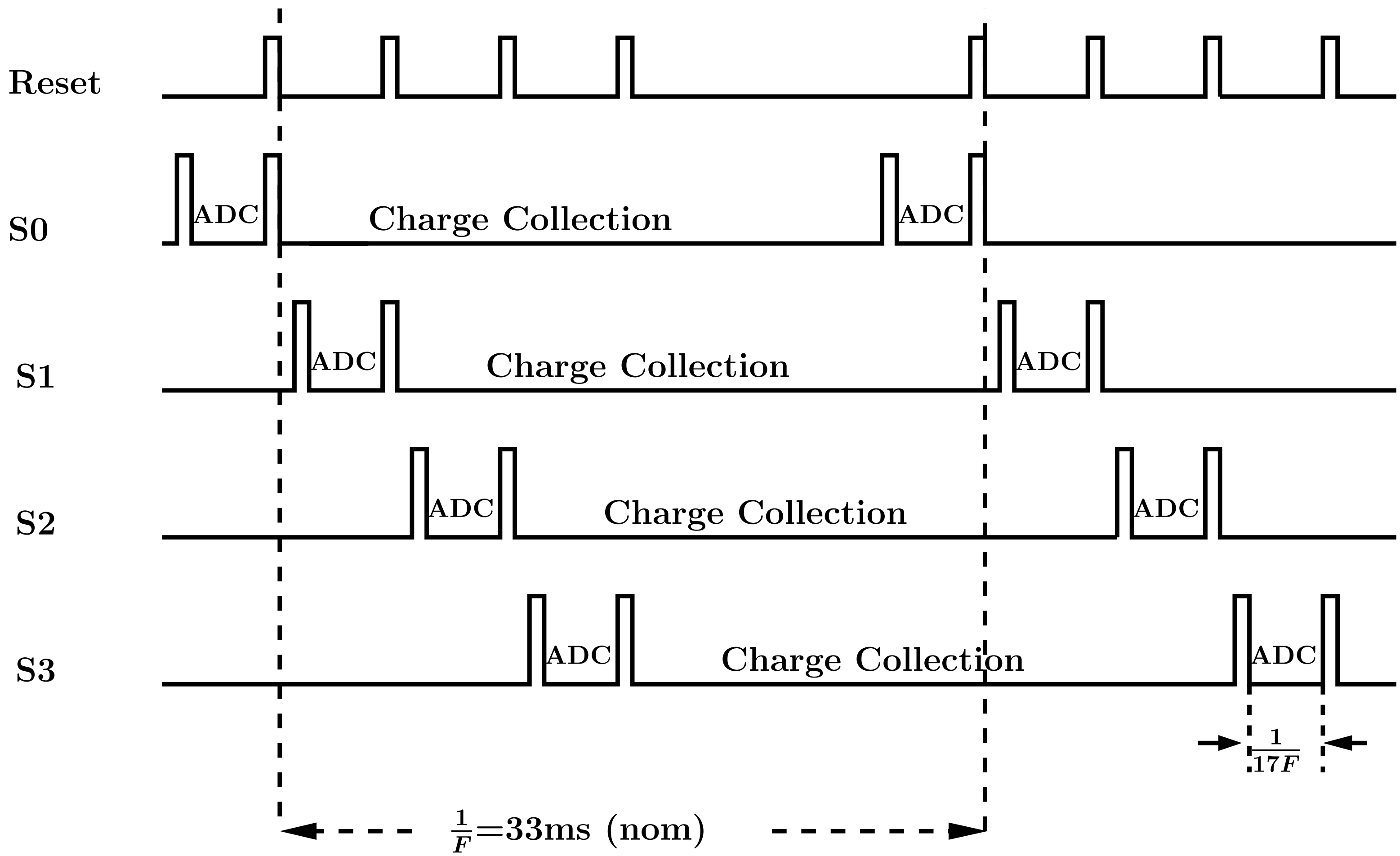
- CICC98, EI99 (invited paper)
- Nyquist rate bit serial ADC
- A/D conversion via successive comparison
- Needs only a 1-bit comparator and a 1-bit latch per pixel block
- ADC shared among a 2×2 pixel block

Mutiplexed MCBS ADC Pixel Block Circuit Schematic



ADC is electrically testable

Timing Diagram of Multiplexed Operation



Signal Transfer Characteristics

Signal path, from photon to digital number, consists of:

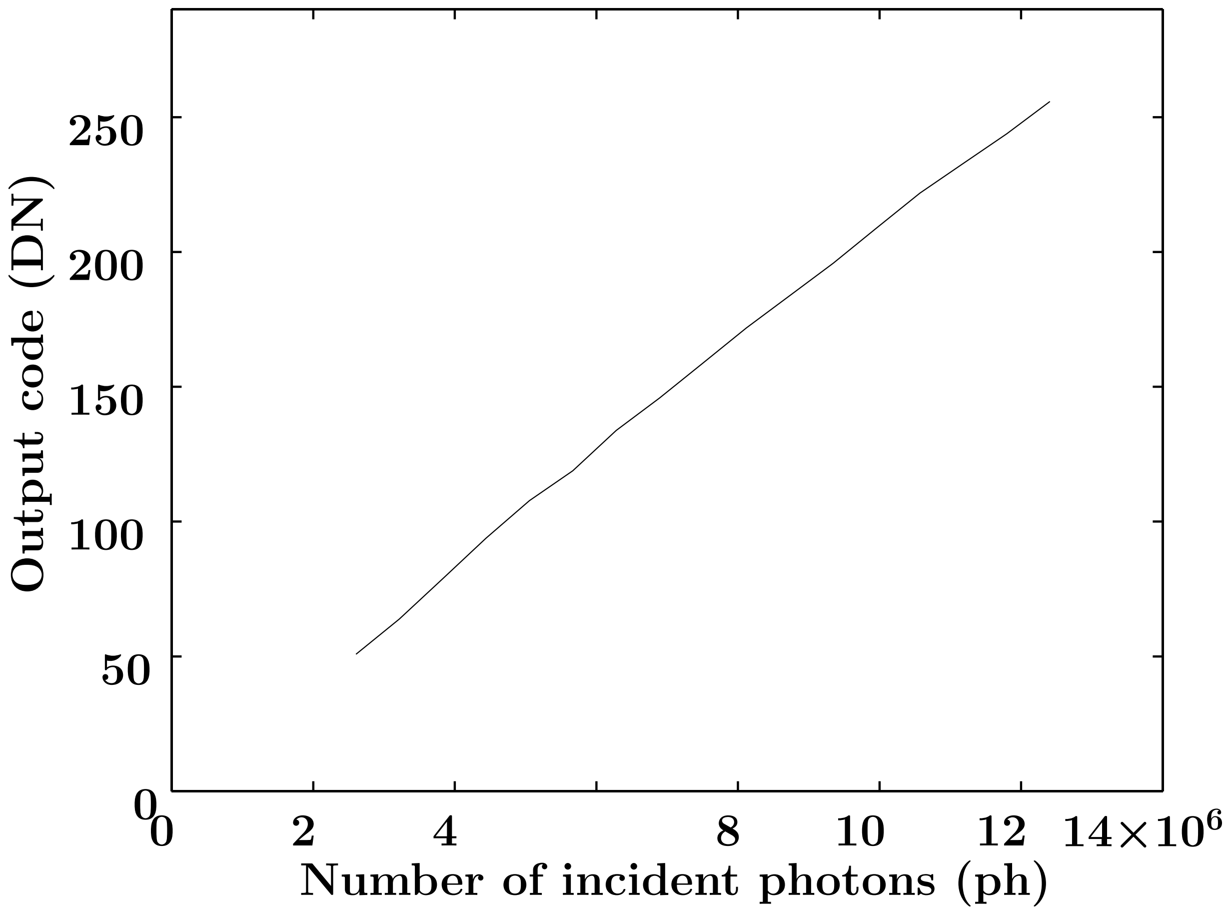
Photonflux $\longrightarrow$ (QE) **Current** $\longrightarrow$ (Integration) **Charge** $\longrightarrow$ (Sensitivity $\frac{1}{C_{sensenode}}$) **Voltage** $\longrightarrow$ (ADC Gain) **DN**

Assuming linearity, signal transfer curve can be characterized by a signal path gain G

$$G = \text{QE} \times \text{sensitivity} \times G_{ADC}$$

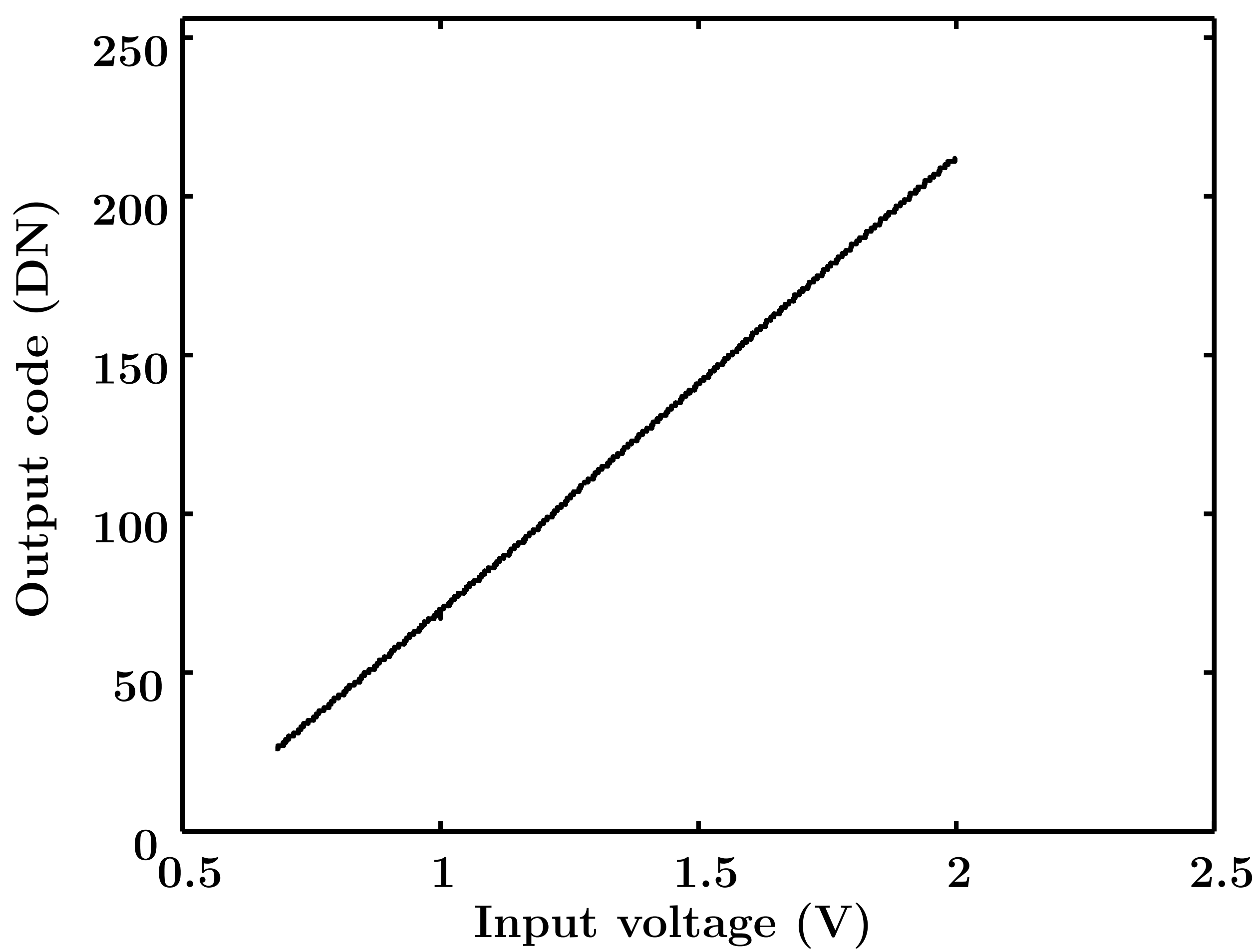
where G_{ADC} is the ADC gain

Signal Path is Linear



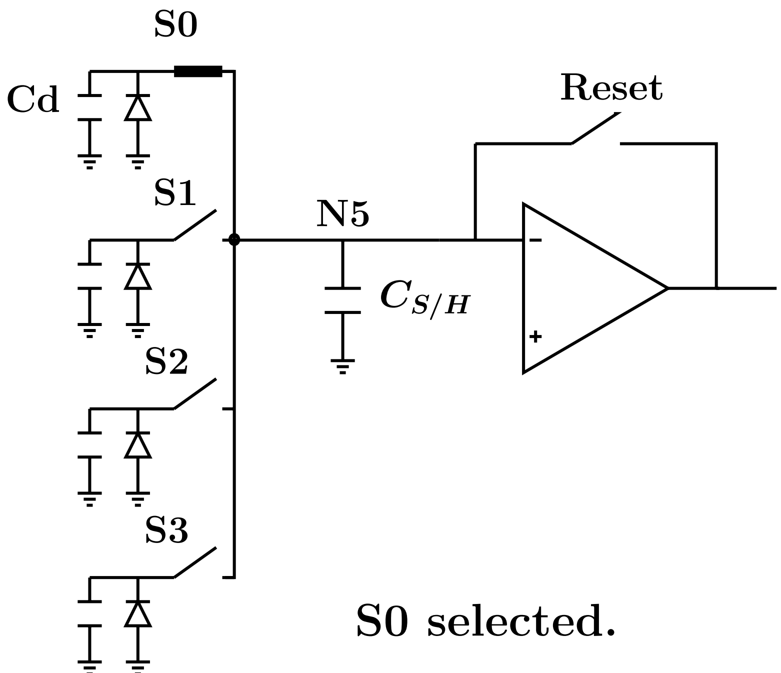
$$G = 2.09 \times 10^{-5}\ \text{DN/ph}$$

ADC Transfer Curve is Linear

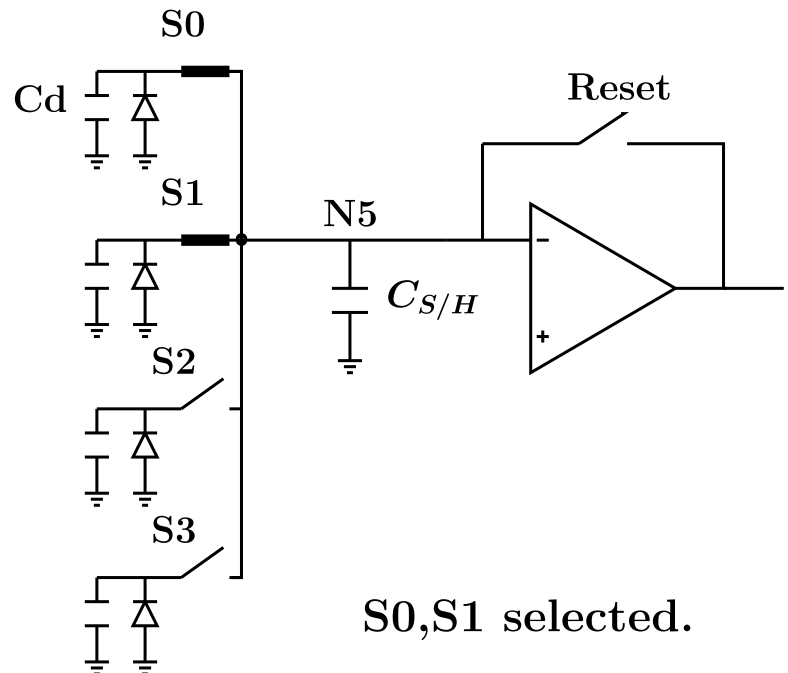


$$G_{ADC} = 128 \text{ DN/V}$$

Sense Node Capacitance Estimation



S0 selected.



S0,S1 selected.

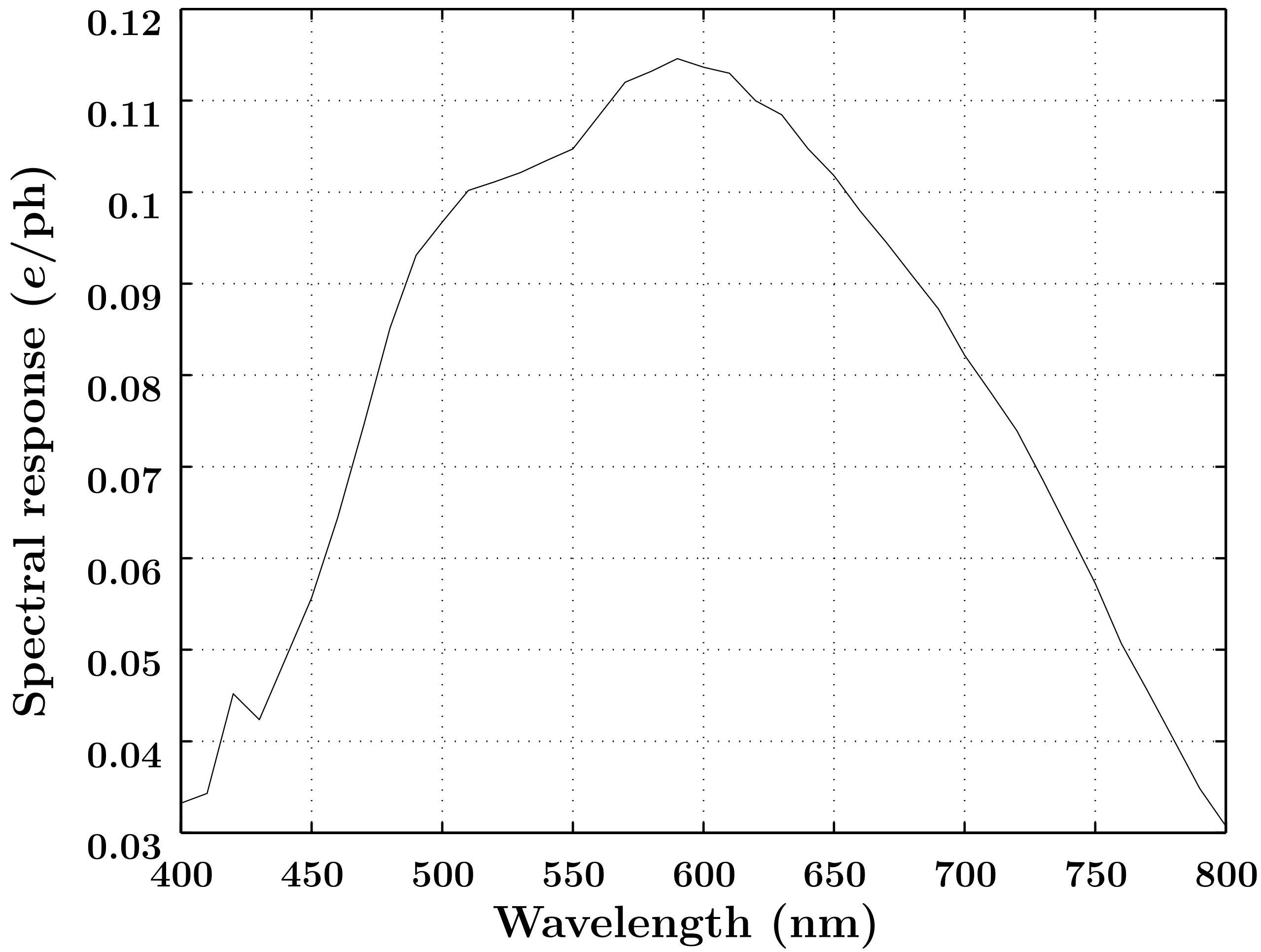
$$(kC_d + C_{S/H})G_k = q\mathrm{QE} \times G_{ADC}, \text{ for } k = 1, 2, 3, 4.$$

Measured Parameters

Sample and hold capacitance	**24.6fF**
Photodetector capacitance	**6.8 fF**
Sensitivity	**5.1 μV/e$^-$**
Signal path gain (G)	**2.09×10^{-5} DN/ph**
ADC gain (G_{ADC})	**128 DN/V**
Quantum efficiency⋆	**11.3% for exposed area and 42% for detector area @ 610 nm**

⋆ 29% of the pixel is exposed to light while the rest is covered by a metal shield. The photodetector itself occupies only 7.8% of the pixel area.

Measured Average Spectral Response



Outline

- Pixel Level ADC Operation
- QE, Sensitivity, and ADC Transfer Curve
- **FPN**

Fixed Pattern Noise (FPN)

- **Pixel output variation under uniform illumination due to device and interconnect variations across the sensor**
- **Measured as the standard deviation of the variations**
- **Magnitude depends on input signal level**

FPN Modeling

For CCD, all pixels share a common amplifier

- **FPN is modeled as a sample from a white noise process**

For CMOS imagers with pixel level ADC, FPN is due to variations among the photodetectors and among the ADCs

- **FPN is the sum of two components photodetector and ADC**

- **Unavoidable quadrant offset due to multiplexing**

FPN Model For Pixel Level ADC

FPN at pixel i, j

$$F_{i,j} = X_{i,j} + \Delta_q + Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}$$

- $X_{i,j}$ – photodetector FPN – white noise process
- $Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}$ – ADC FPN
- $X_{i,j}$ and $Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}$ are uncorrelated
- Δ_q is the quadrant offset, q is the quadrant index

ADC FPN Model

Two dimensional first order isotropic autoregressive process:

$$\boldsymbol{Y}_{\lceil\frac{i}{2}\rceil,\lceil\frac{j}{2}\rceil} = \boldsymbol{a}(\boldsymbol{Y}_{\lceil\frac{i}{2}\rceil-1,\lceil\frac{j}{2}\rceil} + \boldsymbol{Y}_{\lceil\frac{i}{2}\rceil+1,\lceil\frac{j}{2}\rceil} + \boldsymbol{Y}_{\lceil\frac{i}{2}\rceil,\lceil\frac{j}{2}\rceil-1} + \boldsymbol{Y}_{\lceil\frac{i}{2}\rceil,\lceil\frac{j}{2}\rceil+1}) + \boldsymbol{U}_{\lceil\frac{i}{2}\rceil,\lceil\frac{j}{2}\rceil}$$

- $\boldsymbol{U}_{\lceil\frac{i}{2}\rceil,\lceil\frac{j}{2}\rceil}$ **white noise process**
- **Two parameters to be estimated**
  - **correlation parameter –** $\boldsymbol{a}$ $(0 \le \boldsymbol{a} \le \frac{1}{4})$
  - **variance of** $\boldsymbol{U}_{\lceil\frac{i}{2}\rceil,\lceil\frac{j}{2}\rceil}$ **–** $\boldsymbol{\sigma}_{\boldsymbol{U}}^{2}$

Estimated FPN and Autoregressive Parameters

	Dark	30% full well	78% full well
Quadrant offset Δ_q (DN)	0.0	0.01	-3.89
	0.0	-0.10	0.42
	0.0	0.07	1.61
	0.0	0.04	1.86
Photodetector FPN X(DN)	0.0	0.09	2.03
ADC FPN Y (DN)	0.0	0.13	0.06
Total FPN F (DN)	0.0	0.22	2.09

Correlation parameter a	0.02	0.021	0.028
σ_U^2	0.13	0.126	0.058

Conclusion

Methods for characterizing sensitivity, QE, and ADC transfer curve for CMOS imagers with pixel level ADC

Modeling FPN as the sum of photodetector FPN, ADC FPN, and quadrant offset

Design guidelines for pixel level ADC

- **Pixel level ADCs must be electrically testable**
- **Accurate estimate of the sense node capacitance needed for sensitivity**
- **Multiplexing causes offset FPN, but can be corrected digitally.**