Characterization of CMOS Image Sensors with Nyquist Rate Pixel Level ADC

David Yang, Hui Tian, Boyd Fowler, Xinqiao Liu, and Abbas El Gamal

Information Systems Laboratory, Stanford University
Stanford, CA 94305 USA

ABSTRACT

Techniques for characterizing CCD imagers have been developed over many years. These techniques have been recently modified and extended to CMOS PPS and APS imagers. With the scaling of CMOS technology, an increasing number of transistors can be added to each pixel. A promising direction to utilize these transistors is to perform pixel level ADC. The authors have designed and protoyped two imagers with pixel level Nyquist rate ADC. The ADCs operate in parallel and output data one bit at a time. The data is read out of the imager array one bit plane at a time in a manner similar to a digital memory. Existing characterization techniques could not be directly used for these imagers, however, since there is no facility to read out the analog pixel values before ADC, and the ADC resolution is limited to only 8 bits. Fortunately. the ADCs are fully testable electrically without the need for any light or optics. This makes it possible to obtain the ADC transfer curve, which greatly simplifies characterization. In this paper we describe how we characterize our pixel level ADC imagers. To estimate QE, we measure the imager photon to DN transfer curve and the the ADC transfer curve. We find that both curves are quite linear. Using an estimate of the sense node capacitance we then estimate sensitivity, and QE. To estimate FPN we model it as an outcome of the sum of two uncorrelated random processes, one representing the ADC FPN, and the other representing the photodetector FPN, and develop estimators for the model parameters form imager data under uniform illumination. We report characterization results for a 640×512 imager, which was fabricated in a 0.35μm standard digital CMOS process.

Keywords: pixel level ADC, dark current, fixed pattern noise, read noise, QE

1. INTRODUCTION

Techniques for characterizing CCD imagers have been developed over many years. An excellent description of these techniques is provided by Janesick.[1] His paper describes the CCD transfer concept and how it is used to characterize such parameters as charge transfer efficiency, QE, linearity, gain, offset, signal-to-noise, nonuniformity, dynamic range, and MTF. Recently there has been a flurry of CMOS PPS and APS imager design activity.[2–4] Since the signal path for these imagers is quite different from CCDs, the CCD characterization models and techniques cannot be directly used for their characterization. Fowler *et al.*[5] extended the Jansick method to CMOS APS. The modifications account for the nonlinearity, pixel gain variations, and read noise of APS. El Gamal *et al.*[6] proposed to model APS FPN as an outcome of the sum of two uncorrelated components, a column component, and a pixel component. The paper shows how the model parameters are estimated from measurements of the imager outputs under uniform illumination.

With the scaling of CMOS technology, an increasing number of transistors can be added to each pixel without adversely affecting pixel size or fill factor.[7] A promising direction to utilize these transistors is to perform pixel level ADC. Yang[8] describes a 320×256 pixel CMOS imager with pixel level Nyquist rate ADC. A 640×512 version of the imager is described by Yang *et al.*.[9] In both imagers the pixel level ADCs operate in parallel and output data one bit at a time. The data is read out of the sensor one bit plane at a time in a manner similar to a digital memory. Characterizing these imagers, however, is quite challenging. The imagers do not provide any facility for directly reading out the analog pixel values before ADC is performed. In fact it would be very costly in chip area to include analog readout circuitry. Moreover, the resolution

Other author information: Email: dyang@isl.stanford.edu, huitian@isl.stanford.edu, fowler@isl.stanford.edu, chiao@isl.stanford.edu, abbas@isl.stanford.edu; Telephone: 650-725-9696; Fax: 650-723-8473

of the ADC is limited to a maximum of 8 bits, which is adequate for normal image capturing, but is quite inadequate for applying the method described by Fowler *et al.*.[5] The pixel level ADCs, however, are fully testable electrically without the need for any light or optics. This feature, as we shall see, alleviates these characterization challenges.

In this paper we describe how we characterize our pixel level ADC imagers. We show how FPN, QE, spectral response, gain, linearity, dark current, readout noise, and the ADC transfer characteristics are estimated. We report results from characterizing the 640×512 imager.

The remainder of the paper is organized as follows. In section 2 we describe the features of our imager implementation that are most relevant to its characterization. A detailed description of the imager architecture and circuits is provided by Yang[10] and the essential elements of its architecture and operation are provided in an accompanying paper.[7] In Section 3 we describe the experimental setup we used to test and characterize our imager. Section 4 describes how we estimate sensitivity, QE, and spectral response, and provides measured results. Section 5 describes how we modified our FPN model[6] to fit our imager architecture, and provides estimates of the model parameters.

2. PIXEL LEVEL ADC OPERATION

We designed two CMOS image sensors with multiplexed Nyquist rate pixel level ADC, a 320×256 imager and a 640×512 imager. Both imagers were fabricated in a standard digital 0.35μm CMOS process. Table 1 provides the main characteristics for the 640×512 imager. The essential elements of the architecture and operation of these imagers are described in an accompanying paper.[7] In this section we describe the features of these imagers that are most relevant to testing and characterization, specifically multiplexing, autozeroing and electrical testability. A schematic of four pixels sharing an ADC is shown in Figure 2. The four photodetectors are connected to the ADC via an analog multiplexer controlled by **S0, S1, S2 and S3**. All ADCs still operate in parallel but serve one quarter image at a time as shown in Figure 1. Note that there is a timing skew equal to one ADC conversion time between each consecutive quarter images. To achieve reasonably small skew, the ADC time is set to equal 1/17th of the integration time. As shown in Figure 1, before A/D conversion is performed, the charge collected by each photodetector is sampled onto a sample/hold (S/H) capacitor M5. After ADC the sample and hold capacitor and the photodetector are reset via the **Reset** signal, which causes the comparator to operate as an opamp in unity gain feedback. Autozeroing is performed during reset since the comparator offset voltage is stored on the photodetector capacitance in addition to the reset voltage. This autozeroing feature in effect performs correlated double sampling (CDS), which significantly reduces FPN, and 1/f noise. An essential feature to the imager testing characterization is electrical testability. Since the ADC input (node N5 in Figure 2) can be reset to any voltage via **RAMP**, the ADC can be fully tested without any light or optics. To test the ADC, the photodetectors are disconnected by turning off the select transistors. The comparator/latch pair input is then set to the desired **RAMP** value by turning on M4. The set value is then quantized and read out. By stepping the ADC input through its entire input range, the ADC transfer curve can be obtained without any light or optics. This not only greatly simplifies testing of the ADC itself, but also makes characterizing the imager easier, since the only remaining unknown parameters are the photodetector and the S/H capacitances.

3. EXPERIMENTAL SETUP

The 640×512 imager chip has a total of 180 pins, 32 are used to output the digital image data, 17 are used as analog inputs to drive the ADC signals and to set the biases, and the rest of the pins are digital inputs that provide the addresses and other control signals needed for readout. To test and characterize we used the setup shown in Figure 3.

The electrical part of the setup consists of tightly regulated power supplies and two test boards. The first test board is the device-under-test (DUT) board, which includes one plug in socket for the 640×512 imager and another for the 320×256 imager, a 16 bit DAC for generating the **RAMP** signal, and RS422 chips for input and output interfacing. The board also includes level shifters and other analog bias generators to provide the analog input signals to the chip. The output of the DUT board is captured by a PCI digital

Technology	0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS
Sensor size	640 × 512 pixels
Pixel size	10.5 μm × 10.5 μm
Photodetector	n-well to p-sub diode
Sensor area	6720 μm × 5376 μm
Fill Factor	29%
Transistors per pixel	5.5 (22 per four pixels)
Package	180 pin PGA
Supply Voltage	3.3V
Input signal swing	2V
Maximum frame rate	250 frames/s (@ 8-bit resolution)
Dark current	1.3 mV/sec (160 pA/cm^2) at 25°C

Table 1. Main Characteristics of 640x512 Area Image Sensor.

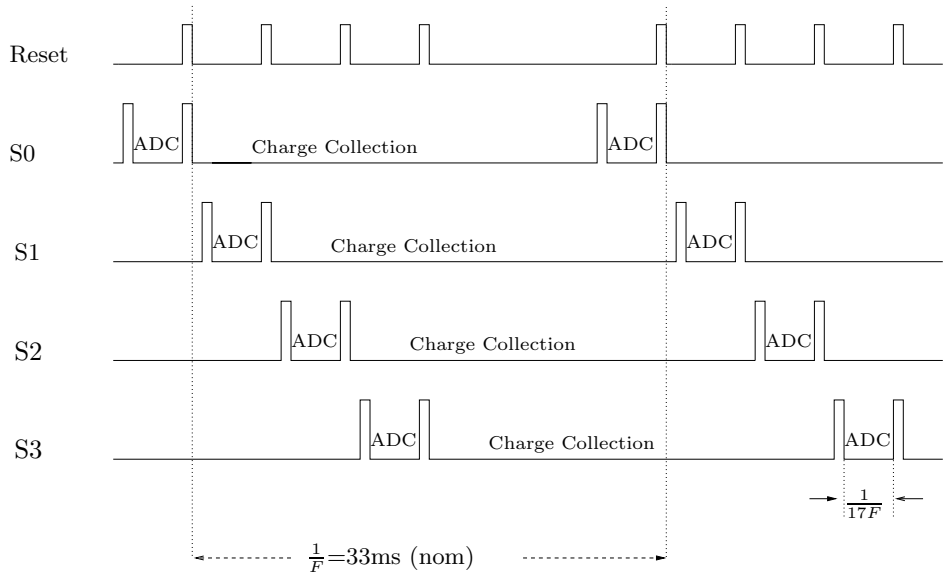

Figure 1. A frame consists of four staggered quarter frames.

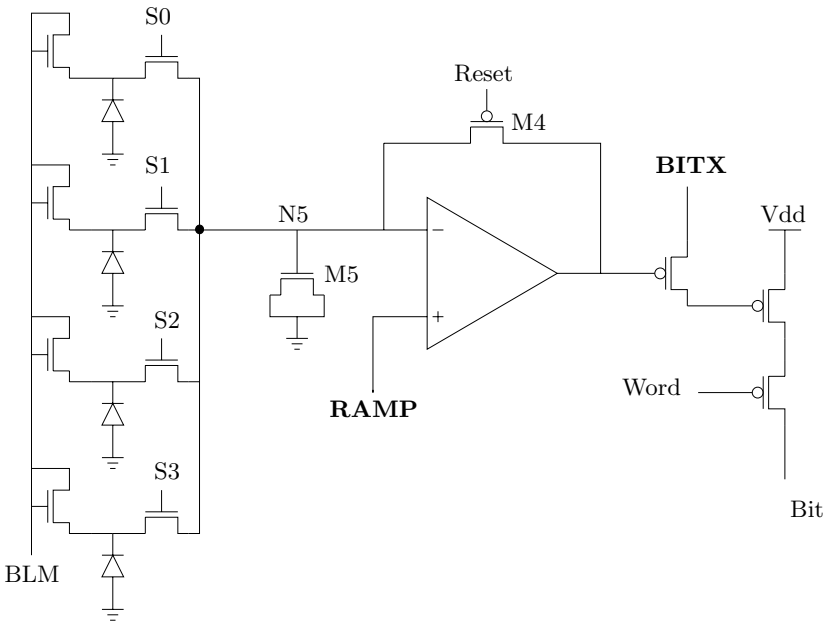

Figure 2. A 2×2 pixel block sharing one ADC.

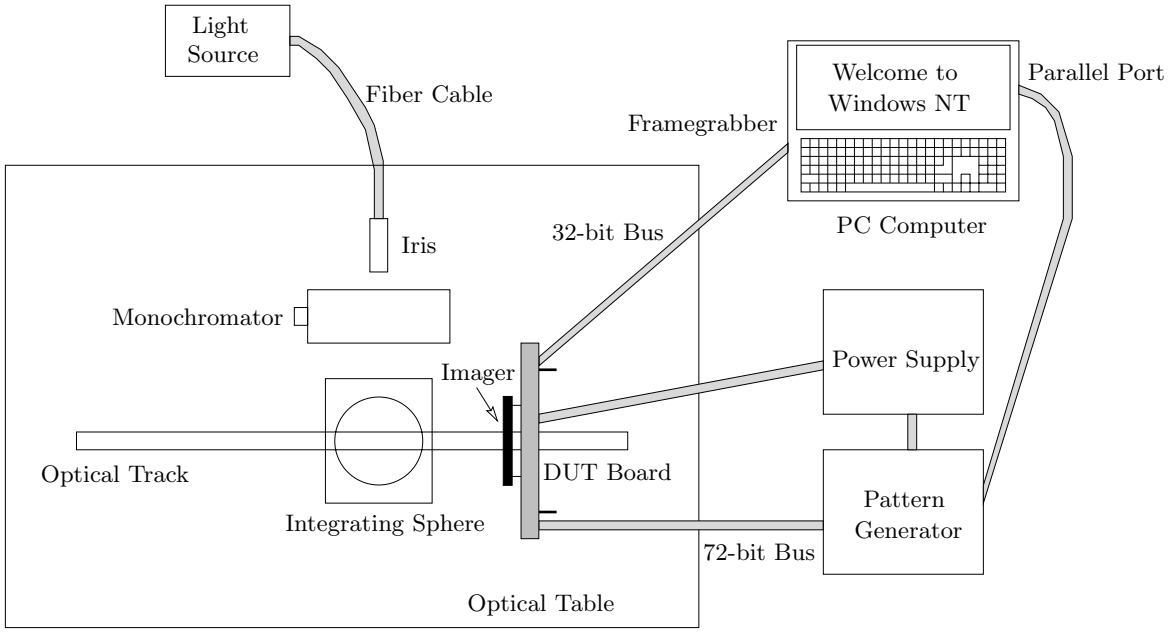

Figure 3. Experimental setup for imager characterization.

frame grabber board that resides in a PC running windows NT. The second board we built is for test pattern generation. The board generates all the needed input patterns to control the imager by driving the digital inputs to the DUT board. The board operates as a special purpose microcontroller featuring a 72 bit wide output bus. The microcontroller is programmed using a very simple assembly language that supports looping and reentrant subroutines. The 72 outputs can be controlled down to the single clock cycle. The microcontroller is implemented using an Actel FPGA and runs at 20MHz. The board is controlled by a PC via its parallel port. To capture data from the imager we first download the appropriate program into the microcontroller memory.

The optical part of the setup consists of a DC regulated tungsten halogen light source, a monochromator, an integrating sphere, and a calibrated photodiode. The monochromator is controlled by a PC. The output of the integrating sphere is used to provide the needed uniform illumination to the imager. All of the electrical equipment and the monochromator are GPIB programmable. We also used a TV optoliner, which is not shown in the figure, to capture test patterns for imager evaluation. The TV optoliner projects a large variety of sharp distortion-free images of selected test pattern directly onto the imager with a high degree of uniformity of light. A full line of neutral density filters allows testing of the imager at extremely low light level. Figure 4 shows an 8-bit image of the EIA 1956 resolution chart obtained from our imager. The image was not corrected or processed before printing.

4. SIGNAL TRANSFER CHARACTERISTICS

To measure the photon to digital number (DN) transfer curve we irradiated the imager with constant monochromatic illumination at 610 nm using the monochromater and the integrating sphere. To find the transfer curve we varied integration time rather than illumination. We read out the imager DN output after 21 linearly increasing integration times 7ms, 33ms, 59ms, ..., and 534ms. The experiment was repeated 256 times and the results were averaged to remove temporal noise. Figure 5 is a plot of the averaged transfer curve for a single pixel. Note that the curve is quite linear. Therefore, we can simply express the signal path gain G_1 (DN/ph) as the product of QE (e^-/ph), sensitivity (V/e^-), and ADC gain G_{ADC} (DN/V). In theory, the ADC gain is entirely determined by the DAC, and is equal to 256 divided by the DAC's input signal swing. The measured DAC's input swing is 2V and its transfer curve shows 16-bit linearity. Therefore, G_{ADC} = 128 DN/V. In practice, however, we must verify that the ADC is linear. To do so we used the electrical testability feature described in section2 to obtain the ADC transfer curve shown in Figure 6. Note that it is quite linear, and that its slope is 136 (DN/V). The discrepancy between the true G_{ADC} = 128DN/V and the measured ADC gain using electrical testing (136) stems from the fact that during electrical testing, resetting introduces charge injection error that is proportional to the reset value. This makes the gain of the measured ADC transfer curve larger than its true value. This effect was verified by switching the select signals to inject varying amounts of charge and observing that the gain varies accordingly.

To estimate QE we need to know the sensor sensitivity. Existing techniques[1,5] estimate sensitivity using shot noise statistics. For these techniques to work the pixel values needs to be quantized to at least 12 bits so that quantization noise is significanly lower than shot noise. Our pixel level ADC produces only 8 bits and it would be difficult to extend its resolution to the needed 12 bits or higher. However, since we already know the ADC transfer curve, the only unknown factor needed to determine sensitivity is the sense node capacitance, which is the sum of the capacitance of the photodetector and its parasitics C_d, and the sample/hold (S/H) capacitor and its parasitics $C_{S/H}$ (see Figure 2). Using the provided process data, we estimated the sample/hold capacitance, which is the gate capacitance of M5, to be 22.6fF and its parasitics to be around 2fF. Thus $C_{S/H}$ is estimated at 24.6fF. Since we used an nwell/psub photodiode no process data was available to us. Fortunately, we were able to estimate the ratio of the two capacitances $\frac{C_d}{C_{S/H}}$ experimentally as follows. We ganged up two photodiodes, by simultaneously turning on **S0** and **S1**, and obtained the signal transfer curve and its corresponding signal path gain G_2. We repeated the experiment by ganging up three photodiodes and then all four photodiodes to obtain the corresponding signal path gains G_3 and G_4. Using the linear capacitor charge to voltage relation we get the four relations $(iC_d + C_{S/H})G_i = k$, for i = 1, 2, 3, and 4, where $k = qQE \times G_{ADC}$. We used least squares to estimate the two unknowns $\frac{C_d}{C_{S/H}}$ and k. The estimate of $\frac{C_d}{C_{S/H}}$ was 0.275, which gives an estimate of the total sense node capacitance $C_d + C_{S/H}$ of 31.37fF and an estimate of the sensitivity of 5.1μV/e^-.

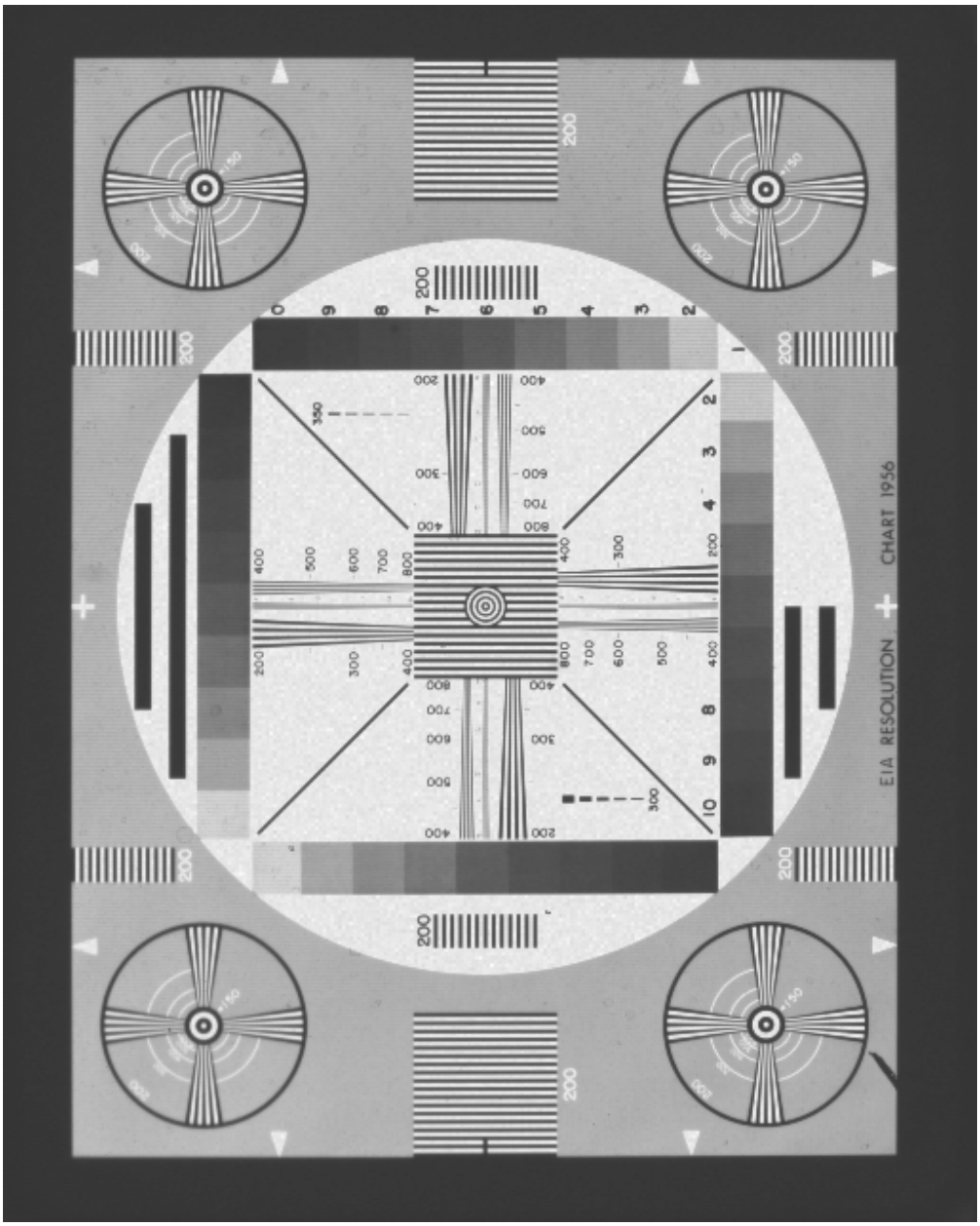

Figure 4. A 640×512 image of the EIA 1956 esolution chart (uncorrected and unprocessed)

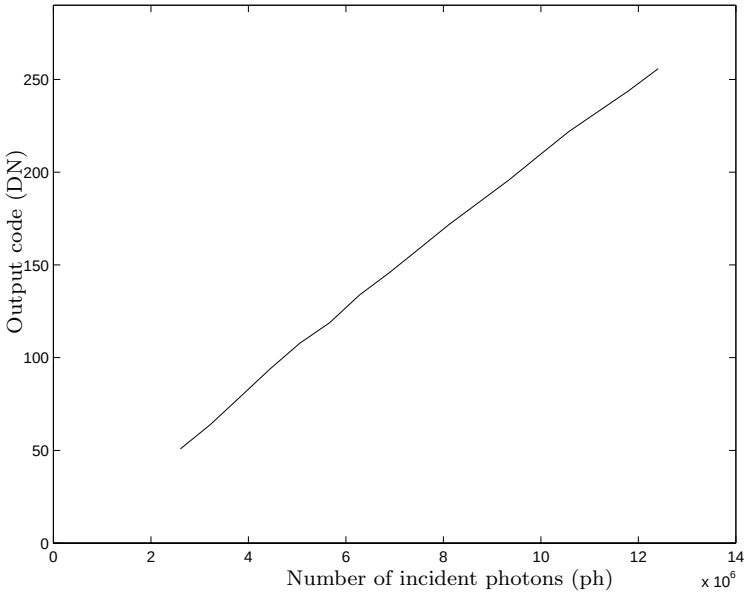

Figure 5. Measured signal transfer curve.

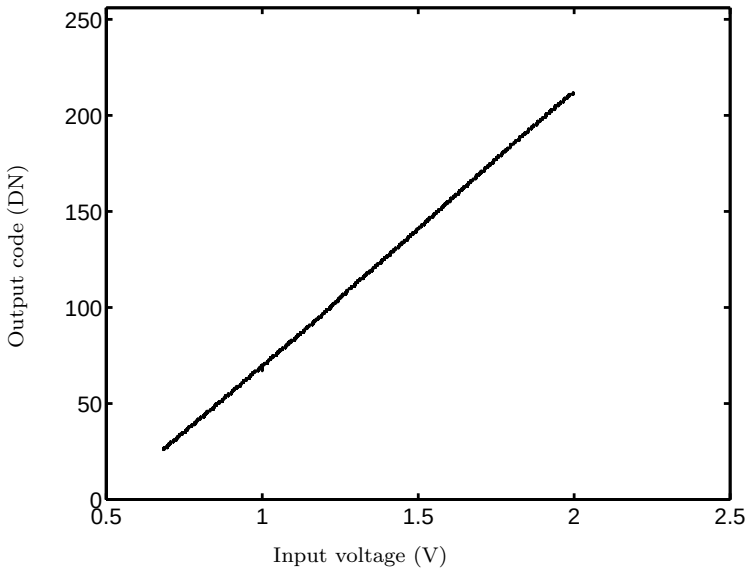

Figure 6. Measured ADC transfer curve.

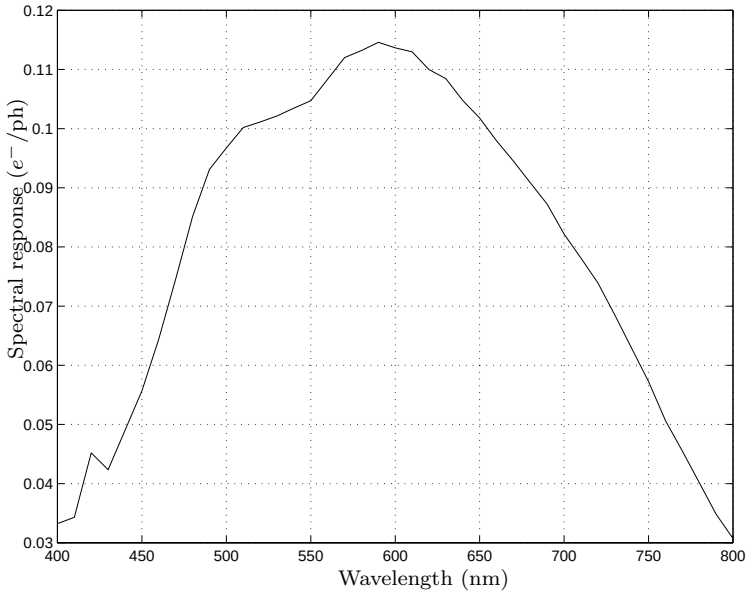

Figure 7. Measured average spectral response of the imager.

Dividing signal path gain G_1 by the product of the estimates of sensitivity and G_{ADC}, we found that QE=3.23%. Since only 29% of the pixel is exposed to light while the rest is covered by a metal shield, QE relative to the exposed area is around 11.3%. Moreover, since the photodetector itself occupies* only 7.8% of the pixel area, QE relative to the photodetector is 36%.

Table 2 summarizes the measured parameters for the 640×512 imager.

Pixel size	$10.5\,\mu$m × $10.5\,\mu$m
Fill Factor	29%
Photodetector area	7.8% of a pixel
Photodetector capacitance	6.8 fF
Sample and hold capacitance	24.6fF
Signal path gain	2.09×10^{-5} DN/ph
Sensitivity	5.1 μV/e$^-$
ADC gain	128 DN/V
Quantum efficiency	11.3% for exposed area and 42% for detector area @ 610 nm

Table 2. Measured parameters of the imager.

The spectral response of the imager was obtained by repeating the procedure we used to estimate QE at different wavelengths. Figure 7 plots the measured average spectral response from 400 nm to 800nm.

5. FPN AND TEMPORAL NOISE

FPN is the variation in output pixel values, under uniform illumination, due to device and interconnect mismatches across an image sensor. In a CCD image sensor FPN is only due to variations in the photodetectors, which are uncorrelated and can thus be modeled as a sample from a spatial white noise process. For a CMOS PPS or APS, there are many more sources of FPN. El Gamal *et al.*[6] model PPS and APS FPN as the sum of two components: a column and a pixel component. Each component is modeled by a first order isotropic autoregressive process, and the processes are assumed to be uncorrelated. For our pixel level ADC imagers FPN is due to the variations among the photodetectors and the variations among the ADCs.

*We used an nwell/psub photodiode. As a result much of the exposed area had to be used to satisfy the well spacing rules.

Photodetector variations is caused not only by the random variations in the photodetectors, but also by the systematic variations due to layout asymmetries resulting from multiplexing. Since each block of 2×2 pixels share an ADC, each quadrant of the imager array is completely symmetrically layed out. However, there are very small, unavoidable, differences between the quadrant layouts, which cause quadrant output offsets. Following a similar methodology to El Gamal *el al.*,[6] we model FPN as an outcome of a two dimensional random process, which is the sum of two uncorrelated processes, one representing the ADC FPN, and the other representing the photodetector FPN. For each quadrant we represent photodetector FPN as an outcome of a white noise process [†] plus a quadrant offset. We assume that the four processes are uncorrelated. We model the FPN due to the ADCs as an outcome of a first order isotropic autoregressive process.

Mathematically, we represent FPN for pixel (i, j) as

$$F_{i,j} = X_{i,j} + \Delta_q + Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}, \tag{1}$$

where q is the quadrant index of the pixel, Δ_q is the quadrant offset, $\{X_{i,j}\}$ is the white noise process representing photodetector FPN, and $\{Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}\}$ is the process representing ADC FPN, which we assume to be a first order isotropic autoregressive process of the form

$$Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil} = a(Y_{\lceil \frac{i}{2} \rceil - 1, \lceil \frac{j}{2} \rceil} + Y_{\lceil \frac{i}{2} \rceil + 1, \lceil \frac{j}{2} \rceil} + Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil - 1} + Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil + 1}) + U_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}, \tag{2}$$

where the $U_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}$s are zero mean uncorrelated random variables with the same variance σ_U^2, and $0 \leq a \leq \frac{1}{4}$ is a parameter that characterizes the dependency of $Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}$ on its four neighbors.

Thus to characterize FPN for our imager we need to estimate the ADC FPN parameters σ_U^2, and a, and the photodetector FPN parameters Δ_q, and $\sigma_{X^q}^2$ for the four quadrants. The $F_{i,j}$s are obtained by reading out the pixel output values multiple times under the same uniform illumination, temporally averaging the values for each pixel to get an averaged pixel value $\bar{V_{i,j}}$, and then subtracting off the overall average pixel output $\bar{V}$ from each $\bar{V_{i,j}}$. Since the ADCs can be directly characterized, the $Y_{\lceil \frac{i}{2} \rceil, \lceil \frac{j}{2} \rceil}$s are obtained by resetting all pixels to $\bar{V}$, reading out the ADC output values multiple times, temporally averaging the values for each ADC, and subtracting off $\bar{V}$. To estimate the model parameters σ_U^2 and a we first estimate σ_Y^2 and covariance $R_Y(1, 0)$ using the estimators given in El Gamal *et al.*.[6] Now we can estimate the photodetector FPN and the quadrant offset as $X_{i,j} + \Delta_q = F_{i,j} - Y_{\lceil \frac{i}{2} \rceil, \frac{j}{2} \rceil}$. Each quadrant offset is estimated as the difference between its average pixel output $\bar{V}^q$ and the overall average pixel output $\bar{V}$, i.e. $\Delta_q = \bar{V}^q - \bar{V}$. The quadrant FPN variances $\sigma_{X^q}^2$ are estimated using a standard variance estimator.

Tables 3 and 4 list the estimated FPN results under dark conditions, and at illuminations corresponding to 30% full well and 78% of full well.

	Dark	30% full well	78% full well
Quadrant offset Δ_q (DN)	0.0	0.01	-3.89
	0.0	-0.10	0.42
	0.0	0.07	1.61
	0.0	0.04	1.86
photodetector FPN X(DN)	0.0	0.09	2.03
ADC FPN Y (DN)	0.0	0.13	0.06
total FPN F (DN)	0.0	0.22	2.09

Table 3. Estimated FPN under dark, 30% and 78% full well signal levels.

In our imager temporal noise is negligible compared to quantization noise. To see this, note that at 8 bits of resolution and assuming 2V of signal swing the standard deviation of quantization noise is around 2.3mV. Our imager has a well capacity of around 90,000 e^-s. Even at the maximum signal value, the shot noise standard deviation is around 300 e^-. Using our sensitivity estimate of 5.1μV/ e^-, the 300 e^- correspond to 1.5mV, which is significantly smaller than quantization noise. Noise from other sources such as KTC, 1/f, etc should be much smaller than 300e^-. Hence, quantization noise dominates. This conclusion is corroborated by measurements of our imager.

[†]This is supported by results for both CCD FPN and PPS pixel FPN.

	Dark	30% full well	78% full well
a	0.02	0.021	0.028
σ_U^2	0.13	0.126	0.058

Table 4. Estimated autoregressive parameters of $Y(i,j)$ (ADC) for dark, 30% and 78% full well signal levels.

6. CONCLUSIONS

We described the methods we used to characterize our Nyquist rate pixel level ADC imagers. We showed how using the electrical testability feature of the ADC, QE can be estimated in spite of the low resolution output of our imager. We proposed a model for FPN as the sum of a photodetector FPN component and an ADC FPN component, and described how the model parameters are estimated from imager data under uniform illumination and ADC data obtained using the electrical testability feature. The FPN model also accounts for the quadrant offsets caused by layout asymmeties due to multiplexing. We presented characterization results from a 640×512 imager fabricated in 0.35μm digital CMOS technology.

Even though the methods and results presented are specific to our imager architecture and implementation there are three important conclusions that should prove beneficial to any imager with pixel level ADC.

- The pixel level ADCs must be designed for electrical testability.
- It is important to obtain an accurate estimate of the sense node capacitance.
- Multiplexing causes almost unavoidable offset FPN. This, however, does not mean that multiplexing should not be used, since the offsets can be digitally corrected for.

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