A 640×512 CMOS Image Sensor with Ultra Wide Dynamic Range Floating-Point Pixel-Level ADC

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Imager Dynamic Range (DR)

- Ratio of largest signal (well capacity) to smallest detectable signal (RMS of read noise)
- Imager DR (especially CMOS) not wide enough to capture both bright and dark areas of scene
- Techniques for enhancing dynamic range:
  - Well capacity adjusting (Decker ISSCC '98)
  - Multiple Sampling
- Multiple sampling achieves higher SNR than well capacity adjusting (Yang SPIE '99)

Multiple Sampling

- Dual sampling: scene imaged twice
  - short exposure time — capture bright areas
  - long exposure time — capture dark areas
- Images combined to form high DR image
- Difficult to implement:
  - high readout speed needed
  - too much data per image — processing needed for reconstruction

Implementing Multiple Sampling in CMOS APS

- APS readout speed limited by settling time of analog signals — cannot even implement dual sampling
- Dual sampling implemented using two column readout ports (Yadid-Pecht Trans. Elec. Dev. '97)
- Dual sampling is not adequate — intermediate illumination areas not well captured by dual sampling
- Extending dual sampling technique to multiple sampling cumbersome

Pixel Level ADC Enables Multiple Sampling

- Signals available to ADCs at all times — can freely choose
  - number and timing of samples
  - number of bits from each sample
- Data read out at fast SRAM speed
- Data rate and external processing significantly reduced

Outline

- **Pixel Level ADC Operation**
  - **MCBS ADC Operation**
  - **Multiple Sampling Operation**
- **A 640×512 CMOS Imager**
- **Experimental Results**

Multi-channel Bit Serial (MCBS) ADC Operation

Complete description in CICC '98

- **Nyquist rate bit serial ADC**
- **A/D conversion via successive comparison**
- **Requires only a 1-bit comparator and a 1-bit latch per pixel or per group of neighboring pixels**

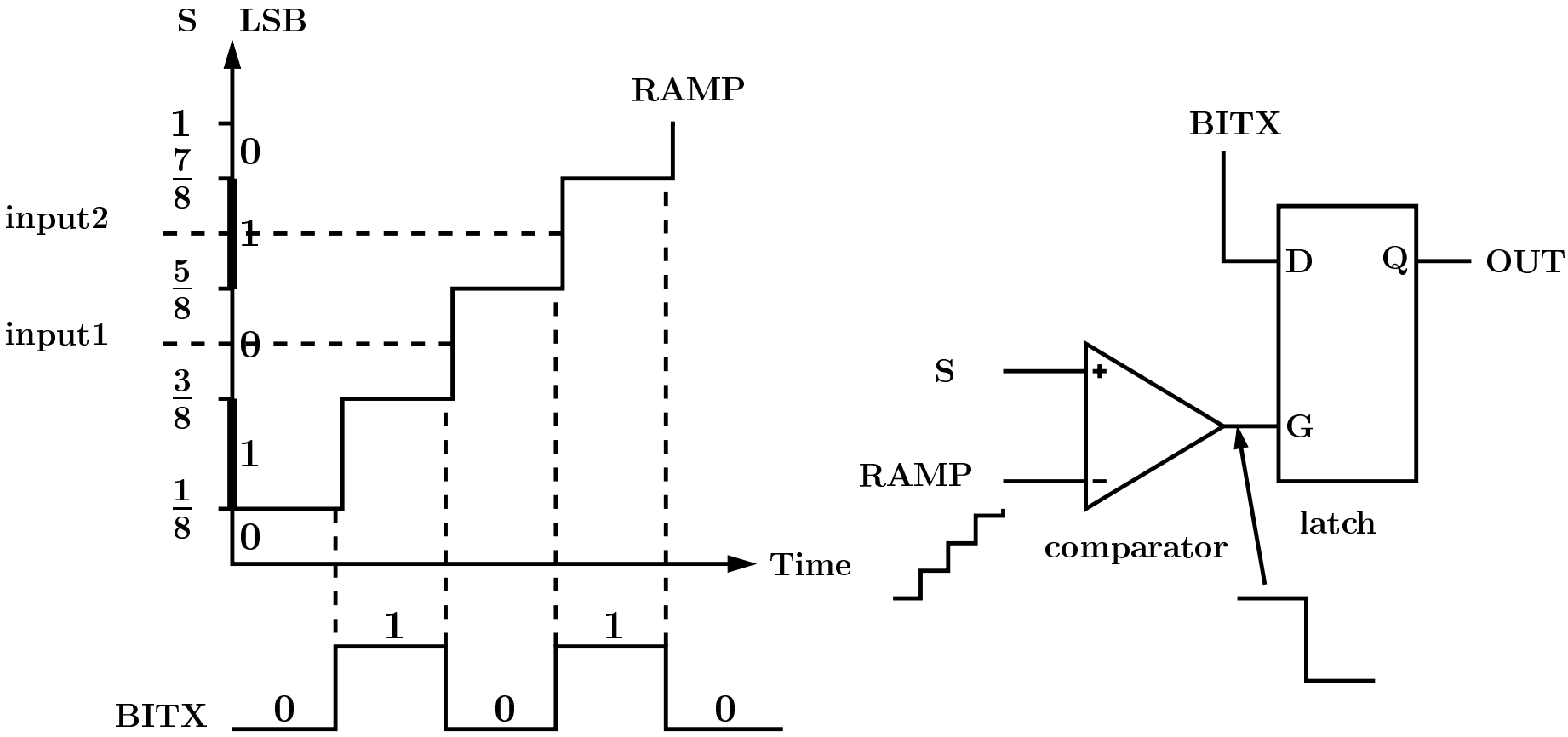
MCBS ADC Method

ADC implements a quantization table

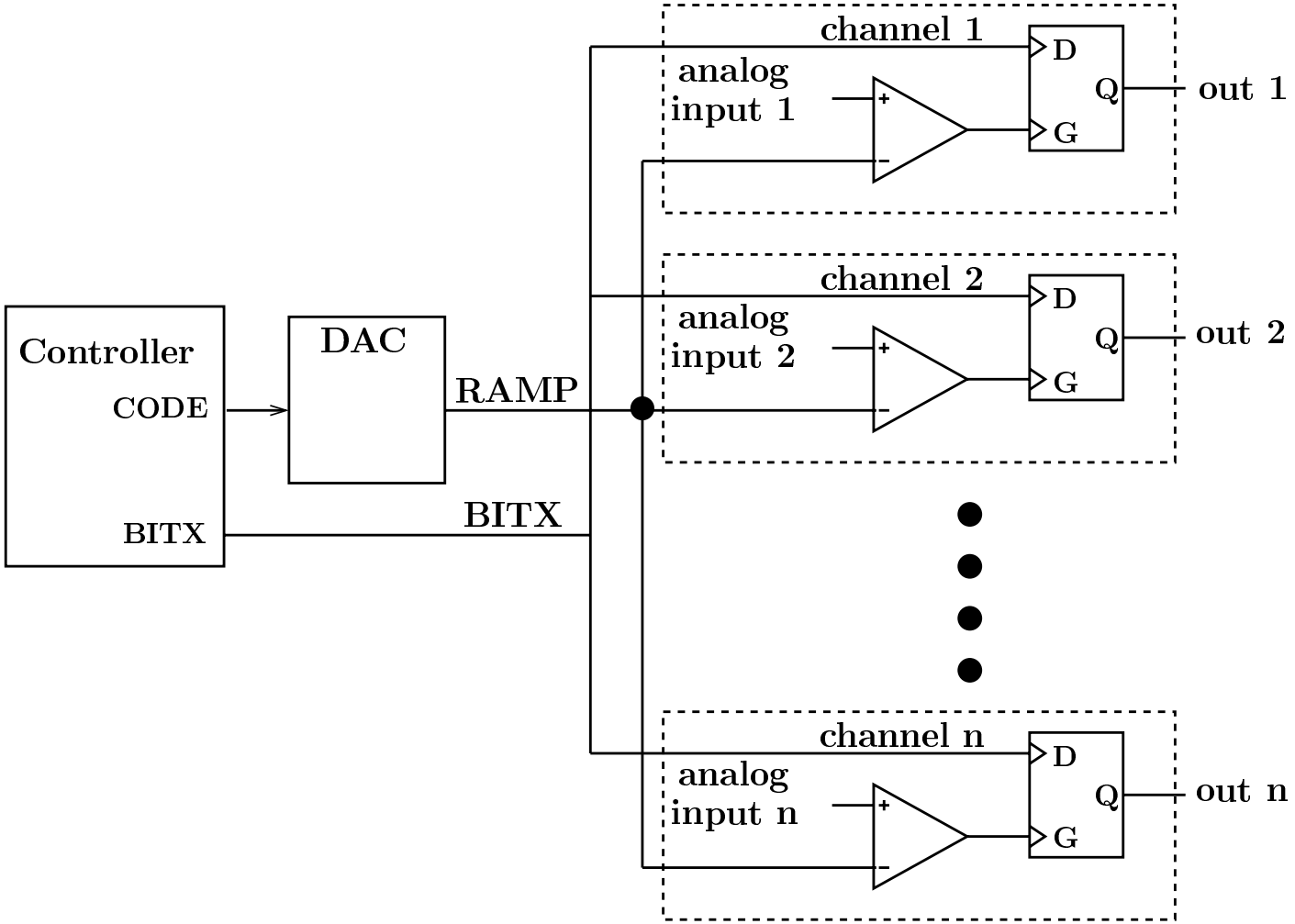
Quantization table	
ADC Input S	**Gray Code**
$0 - \frac{1}{8}$	**0 0 0**
$\frac{1}{8} - \frac{2}{8}$	**0 0 1**
$\frac{2}{8} - \frac{3}{8}$	**0 1 1**
$\frac{3}{8} - \frac{4}{8}$	**0 1 0**
$\frac{4}{8} - \frac{5}{8}$	**1 1 0**
$\frac{5}{8} - \frac{6}{8}$	**1 1 1**
$\frac{6}{8} - \frac{7}{8}$	**1 0 1**
$\frac{7}{8} - 1$	**1 0 0**

Key Point: Each output bit is a function of signal – can be separately generated

How 1-bit Comparator/Latch Works



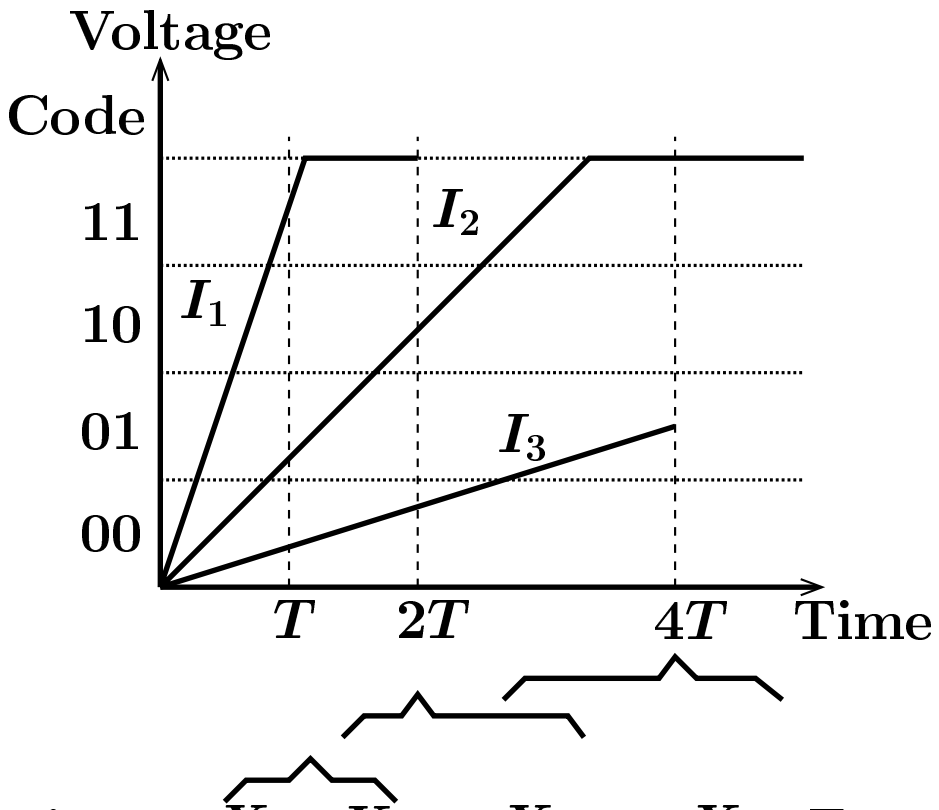
MCBS ADC – Block Diagram



Multiple Sampling Scheme

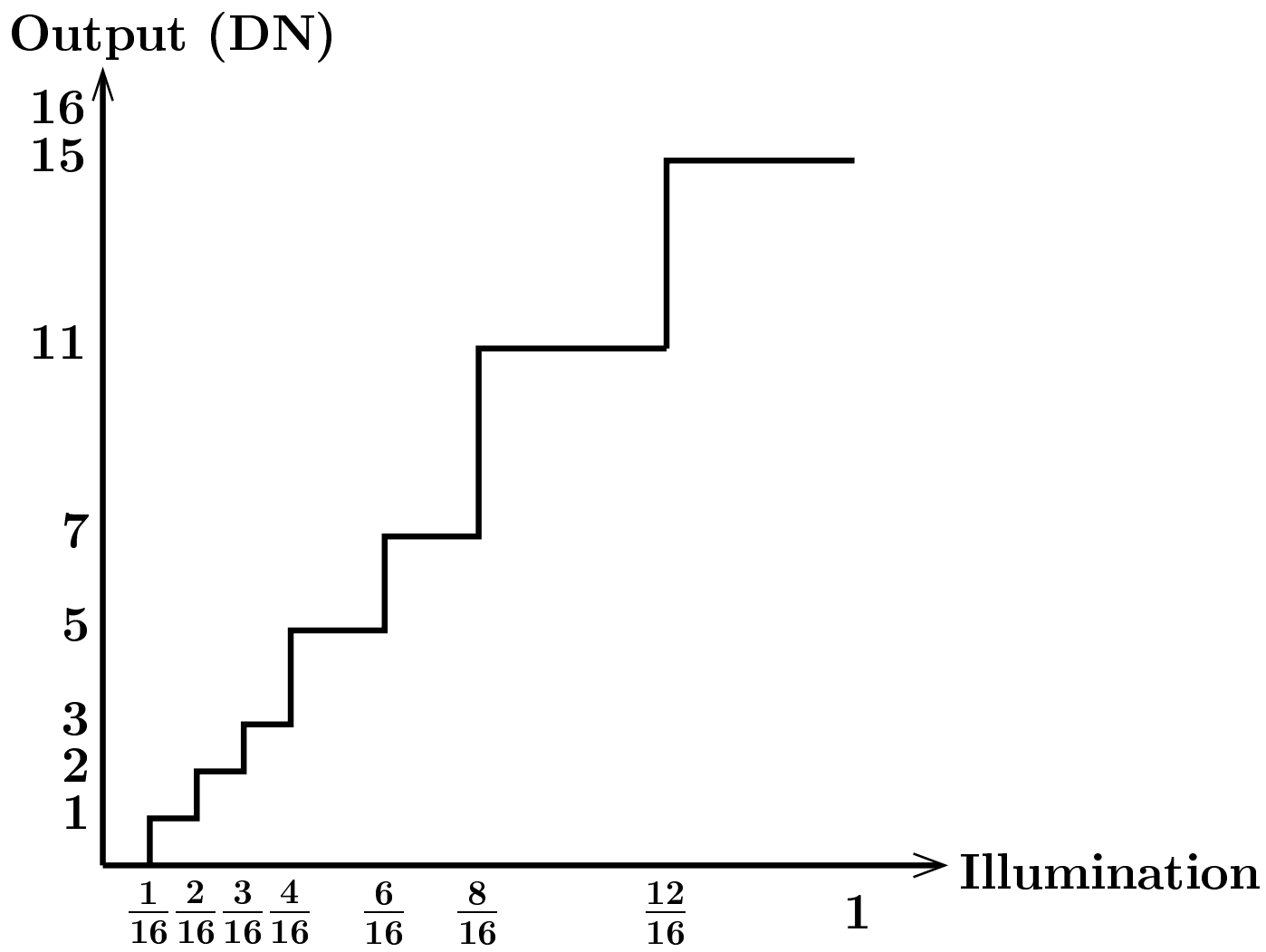
- Scene sampled at exponentially increasing exposure times T, $2T$, $4T$, ... 2^kT
- Each sample is digitized to m bits
- Samples are combined into an $m + k$ bit image with floating point resolution
  - mantissa: m bit
  - exponent: $0, 1, 2, \ldots, k$
- DR is enhanced by a factor of 2^k

Multiple Sampling Example (T, $2T$, and $4T$)



Illumination	X_1	X_2	X_3	X_4	Exponent	Mantissa
I_1	1	1	1	1	2	11
I_2	0	1	0	1	1	10
I_3	0	0	0	1	0	01

ADC Transfer Curve for the $m = 2$, $k = 2$ Example

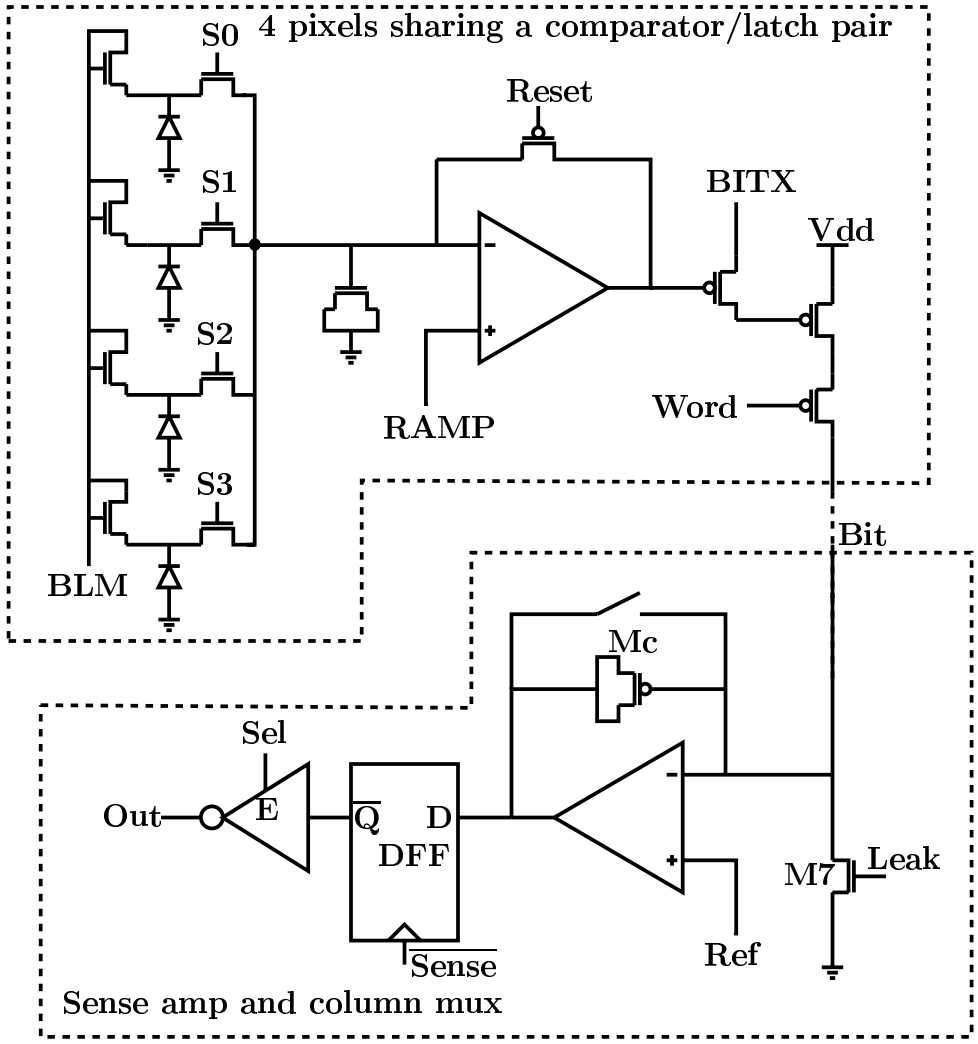


Output is linear function of illumination

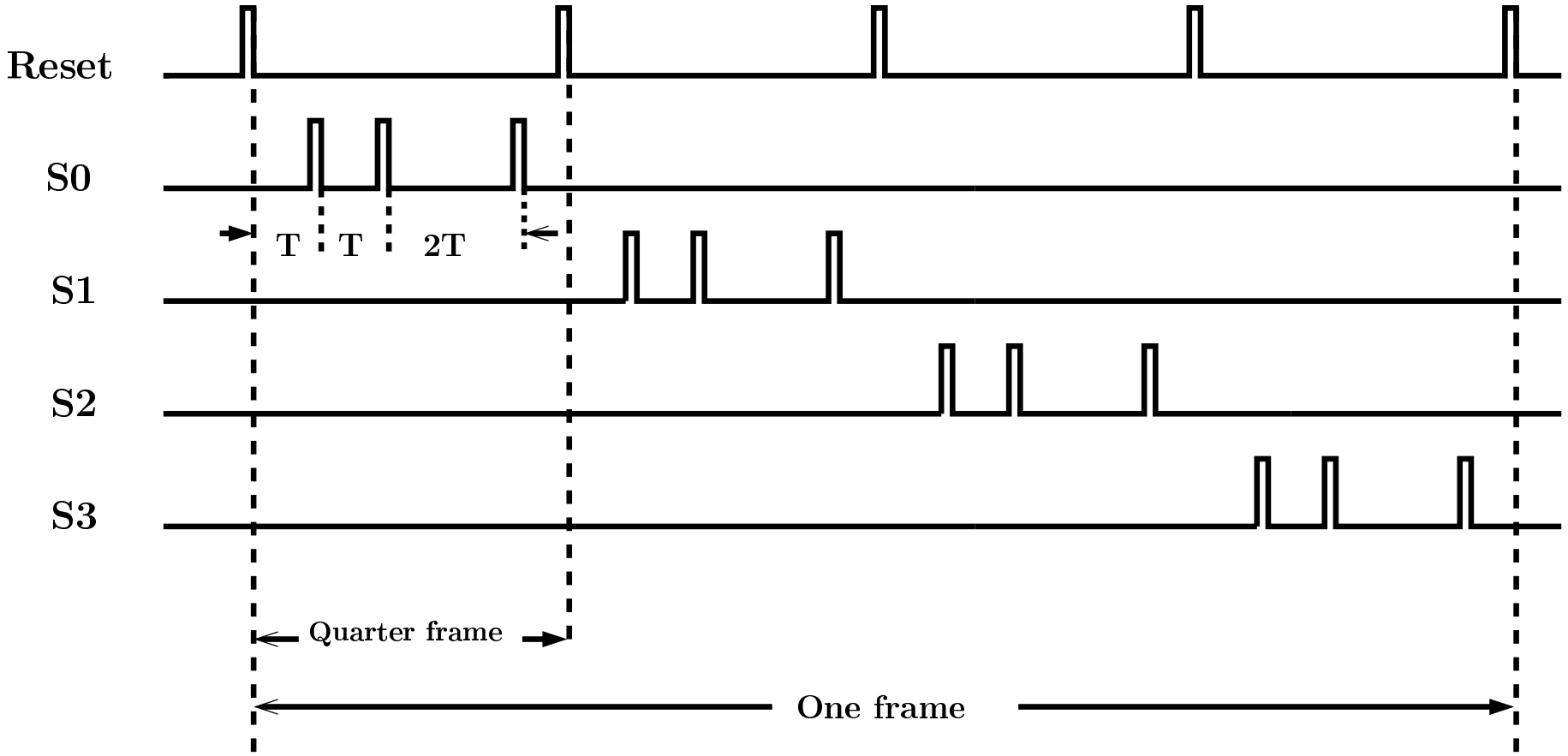
Outline

- Pixel Level ADC Operation
- **A 640×512 CMOS Imager**
  - **Pixel Circuit**
  - **Chip Characteristics**
- Experimental Results

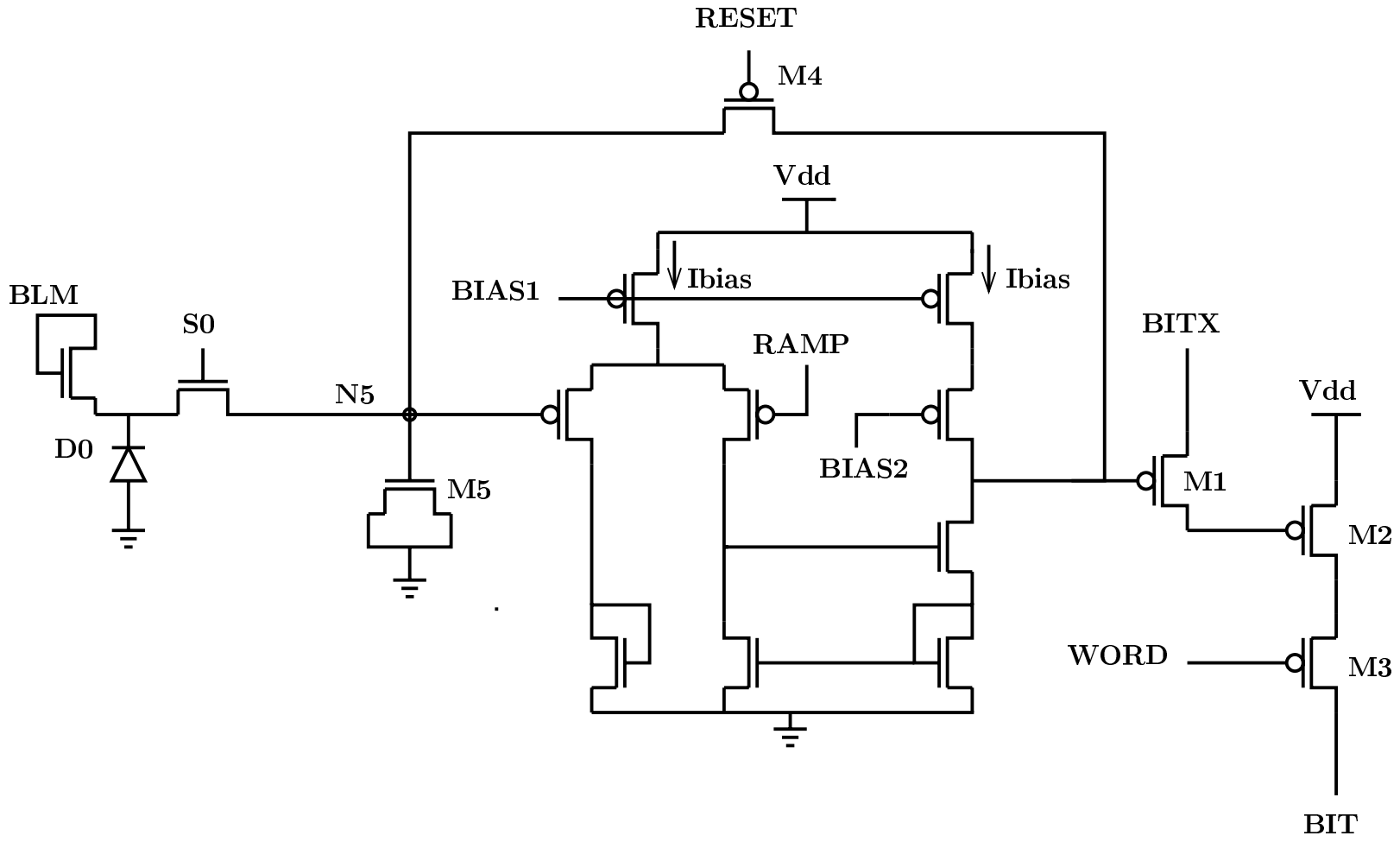
Mutiplexed MCBS ADC Pixel and Column Circuit



Timing Diagram of Multiplexed Multiple Sampling

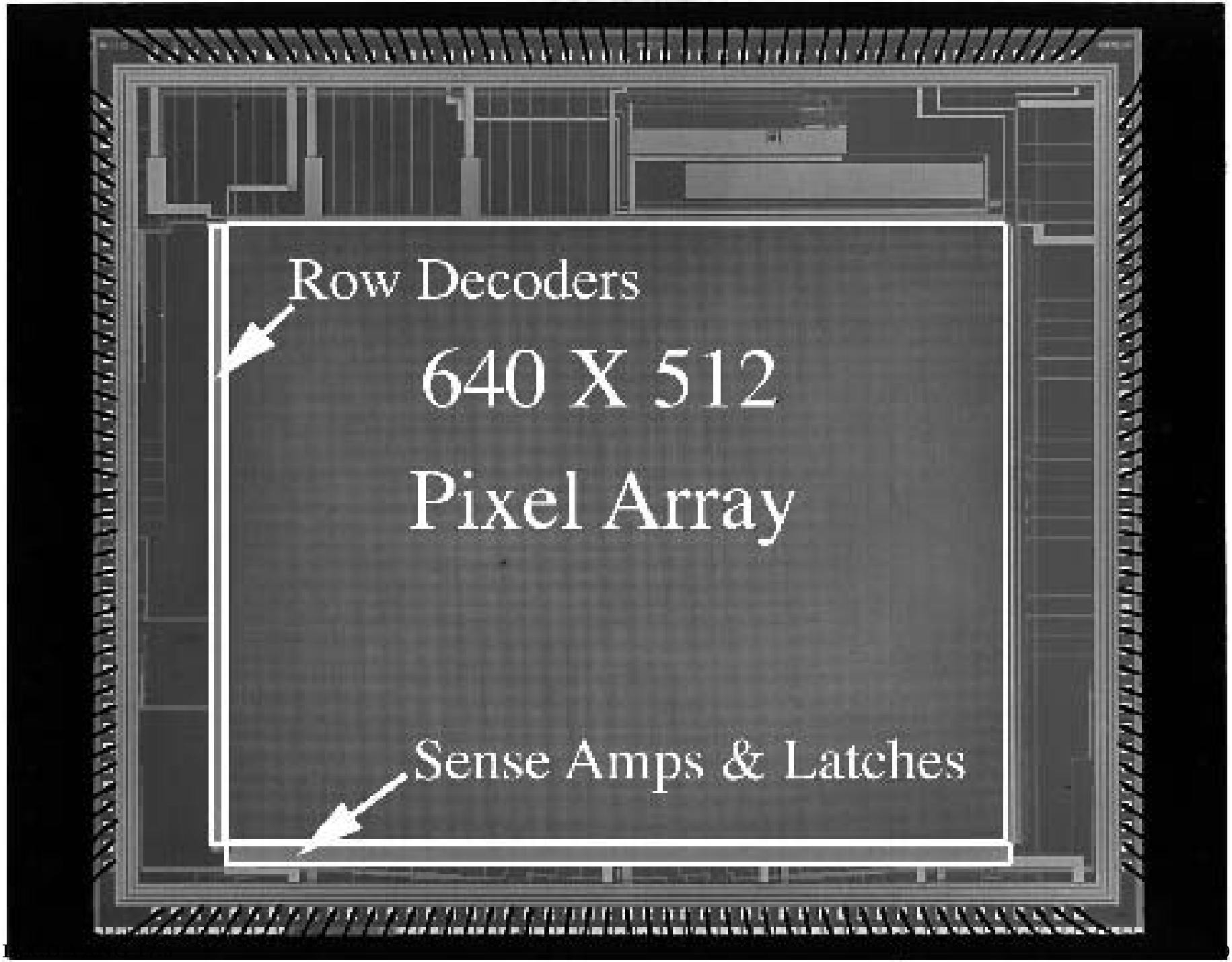


MCBS ADC Pixel Circuit



640×512 Image Sensor Characteristics

Technology	0.35 μm, 1 poly, 4-metal, nwell CMOS
Pixel size	10.5 μm × 10.5 μm
Photodetector	n-well/p-sub diode
Fill factor	29%
Transistors per pixel	5.5 (22 per four pixels)
Supply voltage	3.3V
Package	180 pin PGA
Maximum frame rate	250 frames/s (@ 8-bit resolution)
ADC resolution	8 bit
Sensitivity	5.1 μV/e$^-$
ADC gain (G_{ADC})	128 DN/V
Quantum efficiency	11.3% for exposed area
FPN	0.1 LSB


Row Decoders
640 X 512
Pixel Array
Sense Amps & Latches

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- Pixel Level ADC Operation
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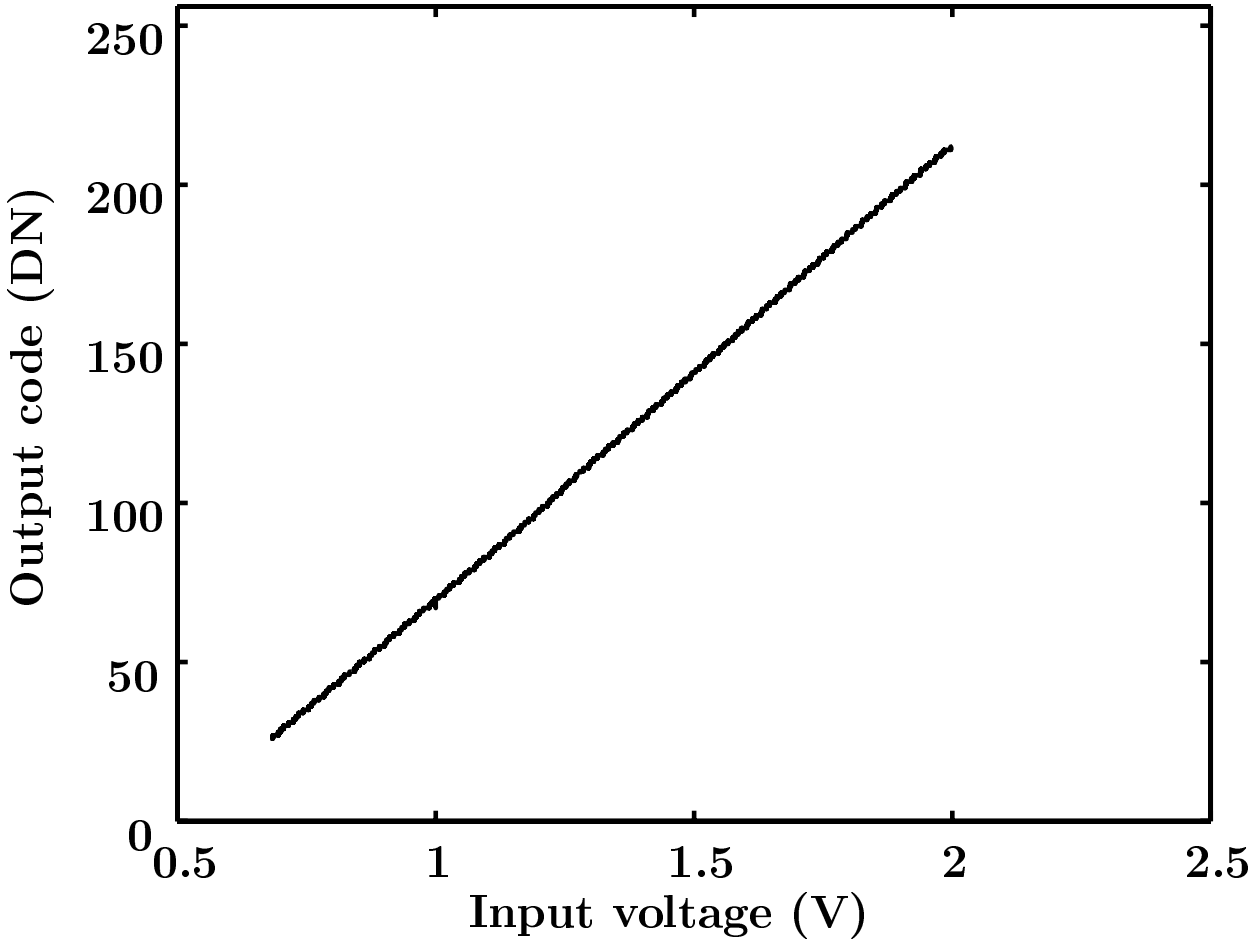
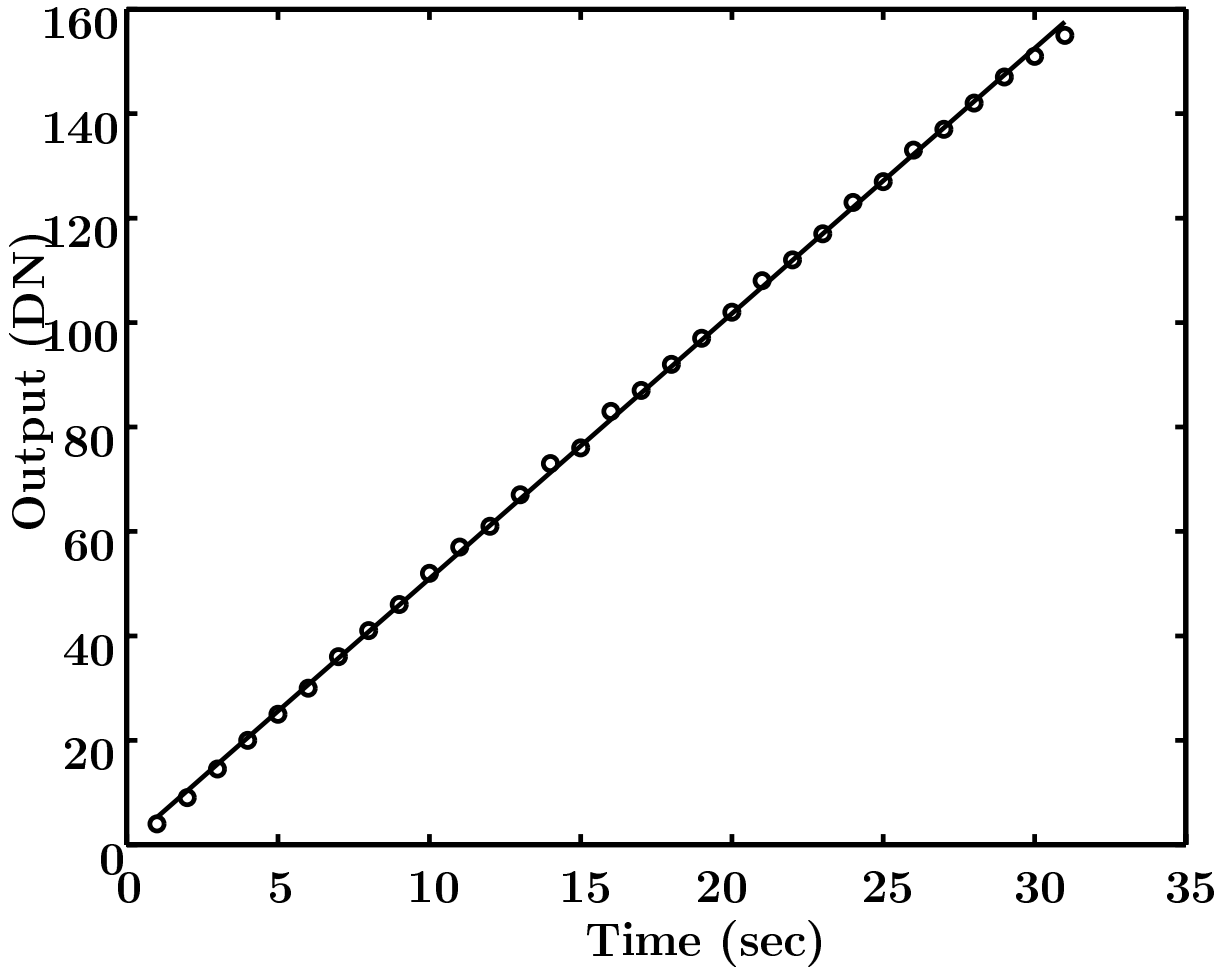
- **Experimental Results**
  - **Signal Transfer Curves**
  - **Multiple Sampling Example**

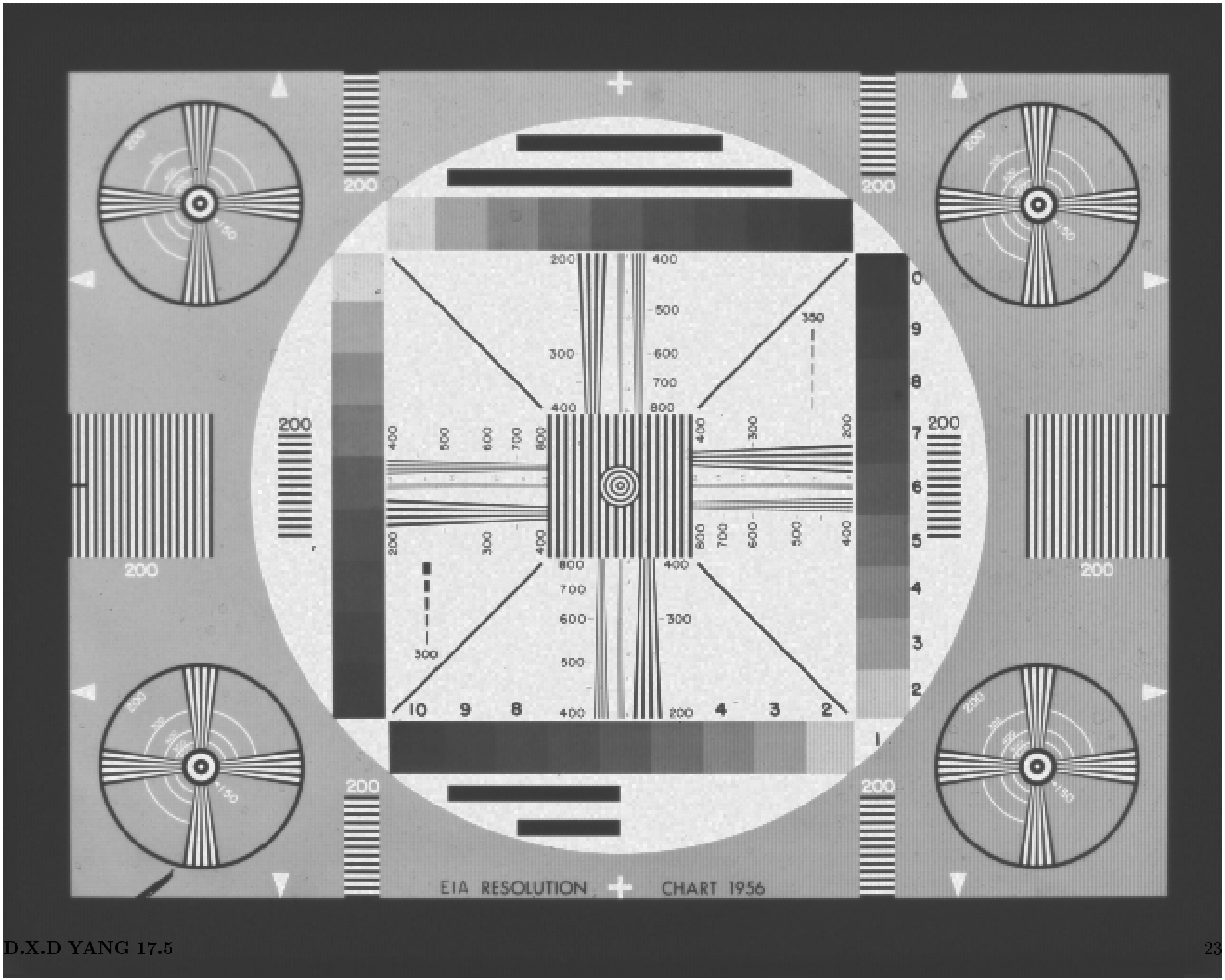
ADC Transfer Curve



$$G_{ADC} = 128 \text{ DN/V}$$

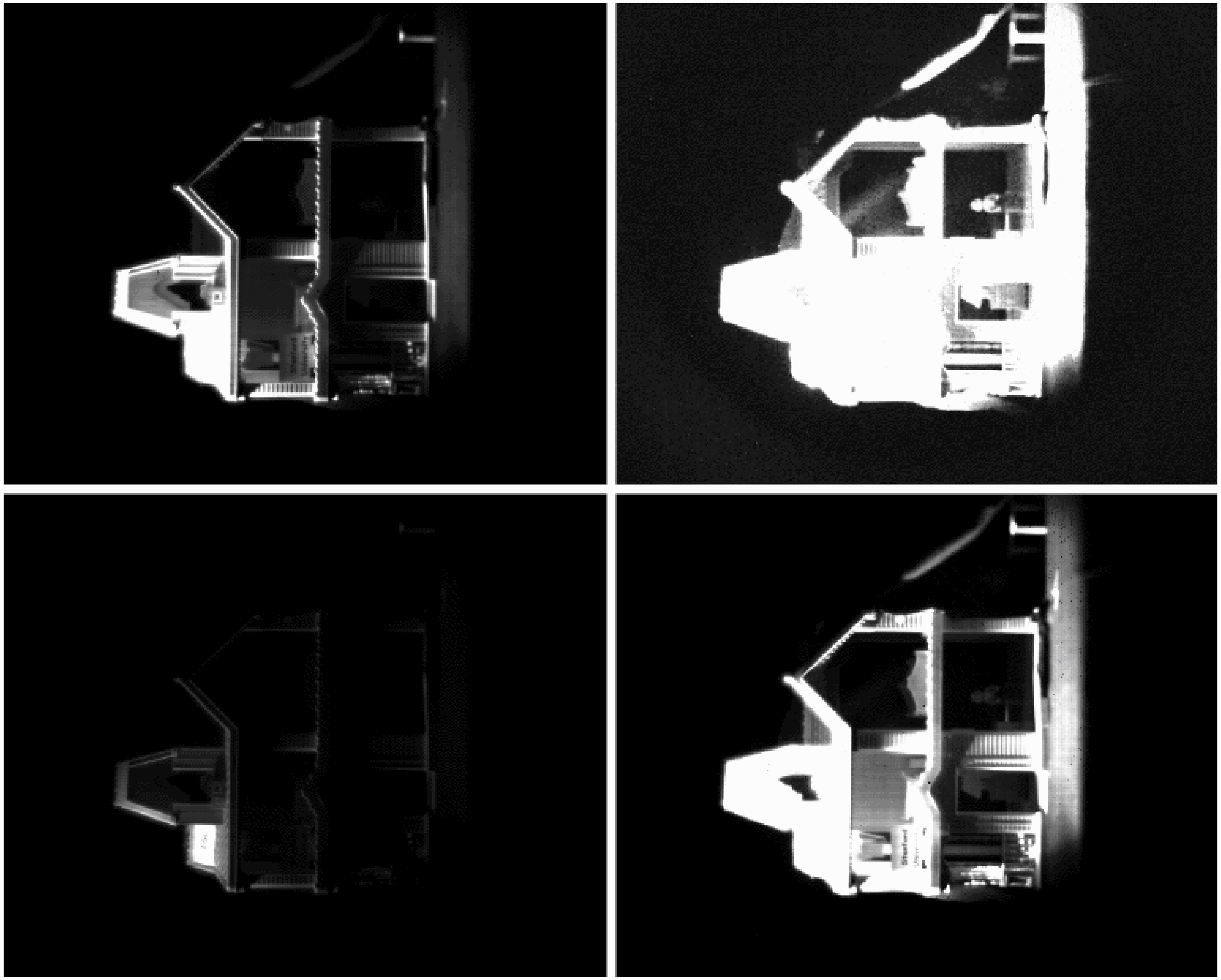
ADC Output vs. Time at Constant Illumination




200
400
500
600
700
800
300
350
10 9 8
4 3 2 1
0 9 8 7 6 5 4 3 2
EIA RESOLUTION CHART 1956

Multiple Sampling of a Dollhouse

- **Scene with dynamic range exceeding 10,000:1**
- **Sampled multiple times at $T, 2T, \ldots, 2^8T$**
- **Obtained a 16-bit image ($m = 8$, $k = 8$)**



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Conclusion

- Pixel level ADC enables implementation of multiple sampling to enhance dynamic range
- Floating point ADC resolution achieved by sampling at exponentially increasing exposure times — output minimum required bits
- Very promising results from a 640×512 pixel imager implemented in 0.35μm CMOS process — 16-bit images
- Another advantage of pixel level ADC — in addition to high SNR, low power, scalability, portability