NOISE ANALYSIS IN CMOS IMAGE SENSORS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF APPLIED PHYSICS
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

By
Hui Tian
August 2000

© Copyright 2000 by Hui Tian
All Rights Reserved

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

Abbas El Gamal
(Principal Adviser)

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

Calvin F. Quate

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

R. Fabian Pease

Approved for the University Committee on Graduate Studies:

Abstract

Digital cameras are rapidly becoming the dominant image capture devices. They are not only replacing film cameras, but also enabling many new applications. Among the most important trends in digital camera design is the use of CMOS image sensors instead of Charge-coupled devices (CCDs). Using CMOS technology enables the integration of capture and processing on a single chip, which reduces system power and cost. CMOS image sensors, however, have lower performance than CCDs mainly due to higher temporal noise and nonuniformity.

Temporal noise sets the fundamental limit on image sensor performance under low illumination and in video applications. In a CCD image sensor, noise is primarily due to the photodetector shot noise and the output amplifier thermal and 1/f noise. CMOS image sensors suffer from higher noise than CCDs due to the additional pixel and column amplifier transistor thermal and 1/f noise, and noise analysis is further complicated by the nonstationarity of the circuit models and the 1/f noise, and the nonlinearity of the charge to voltage conversion.

The thesis presents the first complete and rigorous analysis of temporal noise in CMOS image sensors that takes into consideration these complicating factors. Using time domain analysis, instead of the more traditional frequency domain analysis method, we find that the reset noise power due to thermal noise is at most half of its commonly quoted KTC value. This fundamental result is corroborated by several published experimental data including data collected in our lab. The lower reset noise, however, comes at the expense of image lag. We find that alternative reset methods such as overdriving the reset transistor gate or using a pMOS transistor can alleviate lag, but double the reset noise power. We propose a new reset method that

alleviates lag without increasing reset noise. To analyze the effect of 1/f noise on CMOS image sensors we introduce a nonstationary extension of the recently developed, and generally agreed upon physical model for 1/f noise in MOS transistors. We show that this nonstationary model can be used to obtain accurate estimates of the effect of 1/f noise in switched circuits such as ring oscillators. Using our model and time domain analysis, we find that the conventional frequency domain analysis results using the stationary noise model can be very inaccurate, especially in estimating the 1/f noise effect of the reset transistor.

Acknowledgments

I would like to first and foremost thank my advisor Professor Abbas El Gamal for his invaluable guidance and support, and for encouraging me to perform this thesis work. His insightful and witty comments have made my PhD life very enjoyable. I am grateful to Professor Calvin Quate for being my associate advisor, and for serving on my oral and reading committee. I would like to thank Professor Fabian Pease for serving on my oral and reading committee, and for the helpful discussion that partially led to my work on 1/f noise. I would also like to thank Professor Brian Wandell for chairing my oral committee, and for the enlightening and enjoyable discussions.

From the first day of my PhD research, Dr. Boyd Fowler stands out in helping me intellectually and socially. I thank him for his guidance and help. I also wish to thank Dr. Michael Godfrey for computer and lab support, and for the interesting conversations. Dr. Hao Min also helped me a lot in the image sensor lab and I thank him. I have worked with Dr. David Yang for years, and thank him for the enjoyable cooperation.

My time at Stanford has been intellectually and socially enriched by the friends I have made. I thank all my officemates, T. Chen, S. H. Lim, X. Liu, and K. Salama, for all the helpful discussion and comments, and for the fun activities in and out of the office. I would also like to thank P. Catrysse, J. DiCarlo, R. Erdmann, S. Kleinfelder, and F. Xiao, for the helps and the helpful discussions. I am in debt to L. Lindgren and W. Yu for their great helps.

I wish to thank Professor Geballe for supporting me in the first quarter I came to Stanford. I thank Professor Shen for being my academic advisor during my first two years of PhD study. I appreciate Professor Gill for his help with computer

administration. I thank Charlotte Coe for the help throughout my stay in the research group. I also thank Paula Perron for the administrative work and help.

I would like to thank Analog Devices Inc. and Urbanek family, for supporting me through fellowship. I also thank Agilent, Canon, HP, Interval Research, and Kodak for funding the PDC project, and for supporting me.

Finally and definitely not the lest, I would like to thank my parents, my sister, and my wife for their love and support. I dedicate this thesis to them.

Contents

Abstract **iv**

Acknowledgments **vi**

1 Introduction **1**

1.1 CCD and CMOS Image Sensors 1
1.2 Noise in CMOS Image Sensors 4
1.3 Thesis Organization 7

2 Temporal Noise in CMOS Image Sensors **9**

2.1 Introduction 9
2.2 Mathematical Background 10
2.3 Noise in Integrated Circuits 16
2.3.1 Fundamental Noise Sources 16
2.3.2 Noise Models for Photodiode and MOSFET 18
2.3.3 Analysis of noise in linear circuits 22
2.4 CMOS Photodiode Active Pixel Sensors 26
2.5 Summary 30

3 Analysis of Thermal and Shot Noise in CMOS APS **31**

3.1 Introduction 31
3.2 Noise Due to Reset 32
3.3 Image Lag Due to Incomplete Reset 40
3.4 Noise Due to Integration 44

3.5 Noise Due to Readout 46
3.6 Summary 50

4 Experiments **51**
4.1 Introduction 51
4.2 Experiment Setup and Procedure 52
4.3 Experimental Results 58
4.4 Summary 61

5 MOSFET 1/f Noise Models **64**
5.1 Introduction 64
5.2 Standard 1/f Noise Model 65
5.3 Nonstationary 1/f Noise Model 69
5.4 1/f Noise in a Periodically Switched Transistor 72
5.5 1/f-induced Phase Noise in a Ring Oscillator 76
5.6 Summary 78

6 Analysis of 1/f Noise in CMOS APS **81**
6.1 Introduction 81
6.2 1/f Noise Due to the Follower and Access Transistors 82
6.3 1/f Noise Due to the Reset Transistor 85
6.4 Summary 89

7 Conclusion **91**
7.1 Summary 91
7.2 Future Work and Future Directions 93

Bibliography **95**

List of Tables

4.1 64×64 CMOS APS Test Structure Characteristics. 58

List of Figures

1.1 Digital camera system. 2
1.2 Block diagram of a typical interline transfer CCD image sensors. . . . 2
1.3 Block diagram of a typical CMOS image sensors. 4

2.1 Probability density function of a Gaussian random variable. 12
2.2 Power spectral density of a band-limited white noise process. 14
2.3 Autocorrelation function of a band-limited white noise process. 14
2.4 Waveform of a band-limited white noise process. 15
2.5 Noise model of a thermal noise source. 17
2.6 Noise model of a shot noise source. 18
2.7 Power spectral density of 1/f noise. 19
2.8 Noise Model of photodiode. 19
2.9 Noise Model of MOS transistor. 21
2.10 Integrator circuit. 23
2.11 Linear time invariant circuit. 24
2.12 RC circuit. 25
2.13 A linear time invariant circuit with multiple noise sources. 26
2.14 CMOS photodiode APS circuit and timing diagram. 28
2.15 Noise sources in CMOS APS pixel level circuit. 29

3.1 CMOS APS circuit noise model during reset. 33
3.2 Reset settling time t_{settle} vs. photodiode current. 36
3.3 Simulated photodiode voltage waveform due to incomplete reset. r_1 and r_2 refer to the end of reset for the first and second frames respectively. 41

3.4 pMOS (left) and overdriving gate (right) reset methods. 42
3.5 Pseudo-flash reset method. 43
3.6 Signal voltage vs. photodiode current. 46
3.7 RMS noise voltage vs. photodiode current. 47
3.8 CMOS APS circuit noise model during readout. 48
3.9 Readout noise power spectral density due to M2, M3, and M4. 49

4.1 Experiment setup for CMOS image sensors characterization. 54
4.2 CMOS APS output waveform 59
4.3 CMOS APS output mean as a function of time for segments 1, 2, and 3. 59
4.4 CMOS APS output variance as a function of time for segments 1, 2, and 3. 60
4.5 Simulated vs. measured signal to noise ratio. 62
4.6 Measured final reset voltage for five consecutive frames (indicated by $\times$), and the simulated photodiode voltage waveform (indicated by the dashed lines). 62

5.1 MOSFET with single trap in its gate oxide (top) and the resulting trapped electron number $N(t)$ waveform (bottom). 67
5.2 1/f noise psd as the summation of psds due to multiple traps. 68
5.3 Energy-band diagram for MOSFET, with an active trap inside its gate oxide. Solid lines are used when the transistor is off, and dashed lines are used when the transistor is on. 70
5.4 RMS gate voltage of an nMOS transistor with $1\mu m^2$ channel area (top) and the percentage error using the standard model (bottom). 73
5.5 Spectrum analysis of a periodically switched nMOS transistor. 75
5.6 Simulated 1/f noise psd for switched and dc biased transistors. 76
5.7 The gate voltage of the dominant nMOS transistor in a ring oscillator (top), the associated ISF (middle), and $\alpha(t)$ for $\lambda = 31.6$kHz (bottom). 79
5.8 Simulated 1/f-induced phase noise psd for a ring oscillator. 80

6.1 Small signal model for 1/f noise analysis during readout. 83

6.2 Bitline RMS 1/f noise voltage due to the follower transistor. 86
6.3 Bitline RMS 1/f noise voltage due to the access transistor. 86
6.4 CMOS APS circuit during reset (a), and the corresponding small signal model for 1/f noise analysis (b). 87
6.5 Simulated output referred RMS 1/f reset noise using frequency domain analysis versus using the nonstationary extension and time domain analysis. 89
6.6 Simulated output referred RMS 1/f reset noise using standard 1/f noise model versus using the nonstationary extension, both assuming time varying circuit model. 90

Chapter 1

Introduction

1.1 CCD and CMOS Image Sensors

As more and more people have gained access to the rapidly expanding internet and the ever increasing personal computing power, digital cameras are becoming very popular. Figure 1.1 plots the block diagram of a typical digital camera system. The camera can capture the optical scene and convert it directly into digital format. All the traditional imaging pipeline functions, such as color processing, image enhancement and image compression, can also be integrated into the camera. This enables the quick processing and exchange of images. In addition, they can be made with small size, light weight, low cost, and low power. As a result, digital cameras are quickly replacing traditional film cameras. The unique features of digital cameras also enable many new applications, such as network teleconferencing, video phones, guidance and navigation, automotive applications, and robotic and machine vision, *etc.*

Most of the digital cameras today use the charge-coupled devices (CCDs) to implement the image sensors. Figure 1.2 depicts the block diagram of the widely used interline transfer CCD image sensors. In the CCD image sensors, incident photons are converted to charge and then accumulated by the photodetectors during exposure time. During the following readout time the accumulated charge is sequentially transferred into the vertical and horizontal CCDs, and finally shifted to the chip level output amplifier, where it is converted to voltage signal.

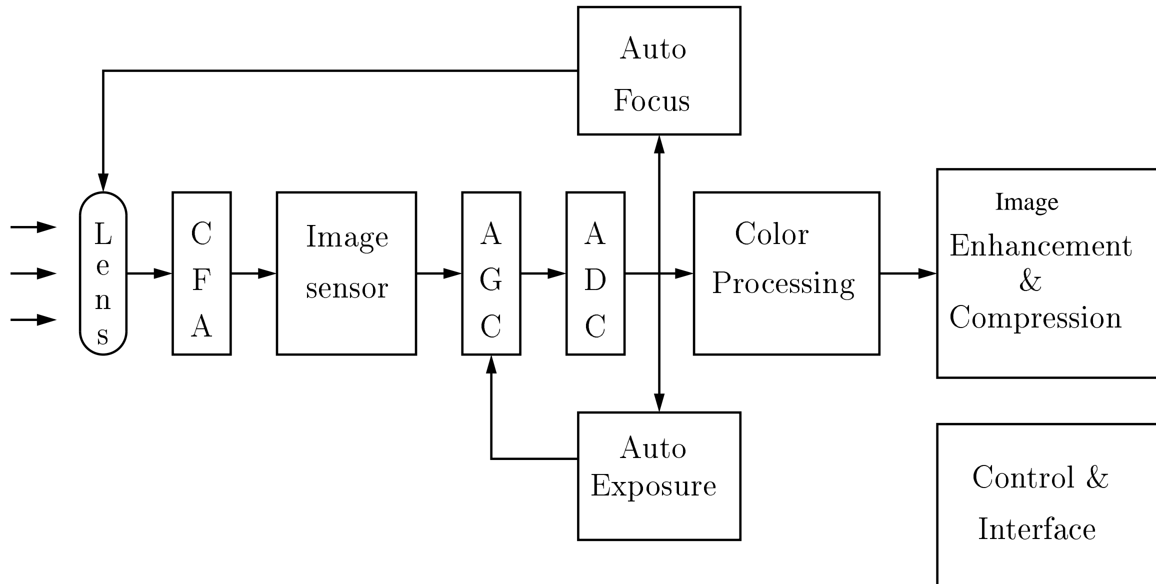

Figure 1.1: Digital camera system.

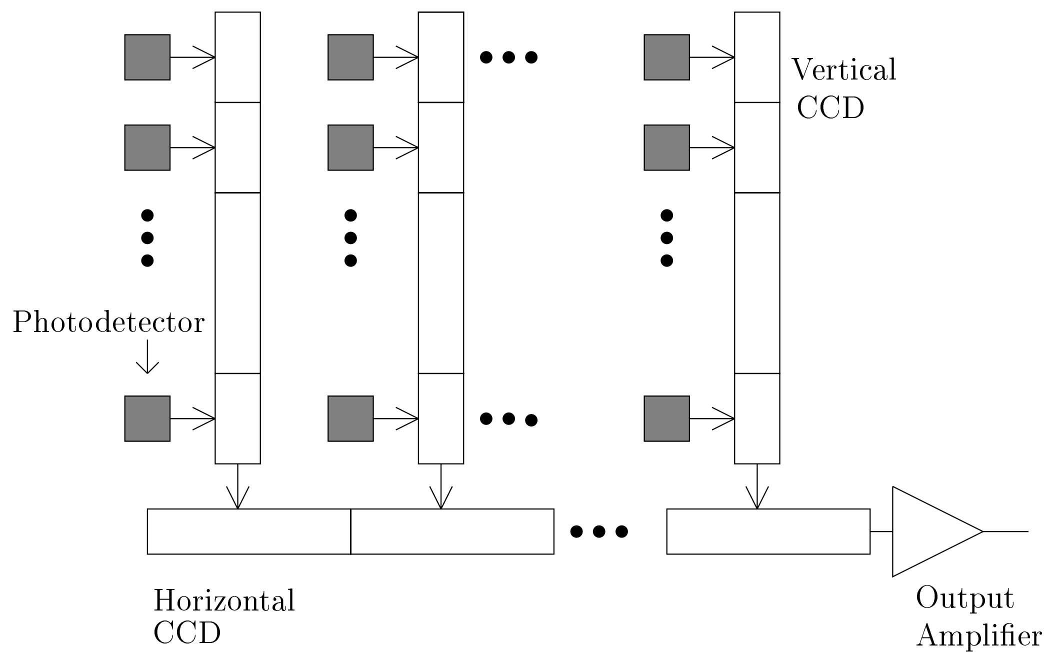

Figure 1.2: Block diagram of a typical interline transfer CCD image sensors.

As the currently dominant image sensor technology used by digital cameras, CCD image sensors can achieve superior noise performance and uniformity, with high fill factor, small pixel size, and large formats. Some limited signal processing operations have also been demonstrated using CCD. The reason that CCD image sensors have low noise and high uniformity is that the charge from every pixel is sequentially converted to voltage signal by the same chip level output amplifier.

However, this sequential readout of pixel charge limits the readout speed. Even worse, because CCDs are high capacitance devices and all the CCDs are switched at the same time with high voltages during readout, CCD image sensors usually consume lots of power. Furthermore, since CCDs cannot be easily integrated with CMOS circuits due to additional fabrication complexity and increased cost, it is very hard to integrate all the camera functions onto a single CCD chip. Instead, multiple chips have to be used. So normally CCD image sensors based digital cameras are relatively large in size and consume high power, and thus are not well suited for portable and embedded imaging applications.

To build portable and embedded imaging systems, it is critical to have the capability of integrating the image sensor together with the circuitry that drives the image sensor and performs on chip signal conversion and processing. This high level of integration not only enables small size of the imaging systems, but also reduces the power consumption and simplifies the system interface. Since Complementary Metal-Oxide-Silicon (CMOS) technology is well suited for implementing on chip signal processing circuits, people start looking at using CMOS technology to implement the image sensors. This leads to one of the most important trends in digital camera design, which is the use of CMOS image sensors instead of CCDs as the imaging devices.

Figure 1.3 plots the block diagram of a typical CMOS image sensors. Unlike CCD image sensors, it adopts a digital memory style readout, using the row decoders and column amplifiers. By doing so, it overcomes many of the problems that CCD image sensors have. Readout now can be very fast and consumes very low power. Random access of pixel values becomes possible, allowing selective readout of windows of interest. Analog signal processing can be integrated onto the same substrate, as

already been demonstrated by some of the video camera systems on a single chip. Analog to digital converters have also been integrated onto the same chip, making it possible to perform the vast variety of digital signal processing and image processing on chip.

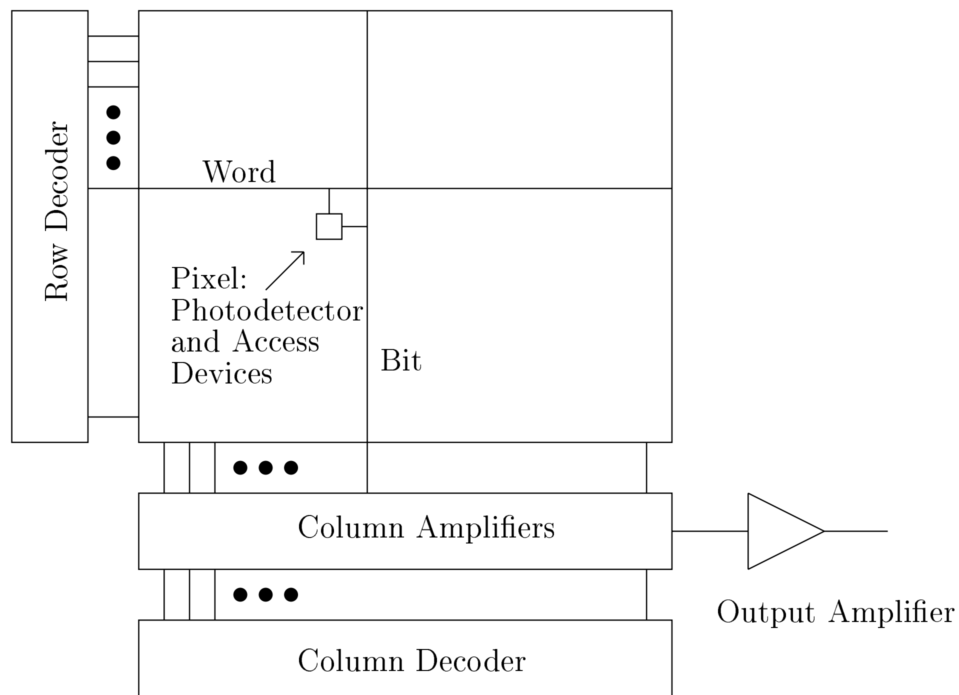

Figure 1.3: Block diagram of a typical CMOS image sensors.

1.2 Noise in CMOS Image Sensors

Despite all the advantages, however, CMOS image sensors have poorer performance when compared to CCD image sensors, and thus have been limited to low end imaging applications so far. Because CMOS image sensors in general have higher temporal noise, higher fixed pattern noise, higher dark current, smaller full well charge capacitance, and lower spectral response, they cannot provide the same wide dynamic range (DR) and superior signal to noise ratio (SNR) that the CCD image sensors enjoy. To

see why this is the case, we briefly go over the history of CMOS image sensors here. A detailed review of CMOS image sensors, including their ancestor MOS image sensors, can be found in [10, 11] by Fossum.

Although MOS image sensors first appeared in the late 1960s [55], most of today's CMOS image sensors are based on the study around the early 1980's. During that time passive pixel sensor (PPS) was the CMOS image sensor technology of choice [8, 9, 39, 37, 38], which contains a photodetector and a single pass transistor within each pixel. Charge sensing is used to readout the signals.

In the early 1990s active pixel sensor (APS) [10, 33, 32] becomes popular. In contrast to the PPS approach that uses a simple switch to connect the pixel signal charge to the column bus capacitance, APS adds some more active transistors to each pixel. The in pixel active transistors can provide both gain and buffering functions, and thus achieve lower noise readout, improved scalability to large array formats, and higher speed readout, compared to PPS. With the advent of deep submicron CMOS technologies and microlenses, APS has now become the CMOS image sensor technology of choice [30, 46, 36].

Most recently digital pixel sensor (DPS) [13, 58, 60] emerges. Unlike APS and PPS, where the analog to digital (A/D) conversion is performed at chip level or column level, DPS integrates an A/D converter into each pixel. By performing the A/D conversion in parallel for all pixels, the DPS holds the promise of even faster operation, lower power, and higher SNR, when compared with APS.

Because each pixel contains one or more transistors, fixed pattern noise (FPN) had been the primary concern for CMOS image sensors. This was also one of the major reasons that helped CCD image sensors to become the dominant solid state imaging technology. Fortunately the development of both on chip signal processing, mainly the correlated double sampling (CDS) technique, and off chip digital signal processing (DSP) have helped to reduce the FPN to acceptable range.

However, temporal noise performance of CMOS image sensors still lag behind CCD image sensors. Since it sets the fundamental limit in sensor dynamic range, and reduces the sensor signal to noise ratio especially under low light conditions, high end imaging applications usually have abandoned CMOS sensors so far. Thus a fully

understanding of noise mechanism in CMOS image sensors becomes necessary, and is essential to guide the development of the next generation of CMOS image sensors.

In a CCD image sensor, temporal noise is well studied and characterized. It is primarily due to the photodetector shot noise and the output amplifier thermal and 1/f noise. CMOS image sensors suffer from higher noise than CCDs due to the additional pixel and column amplifier transistor thermal and 1/f noise, and noise analysis is further complicated by the nonstationarity of the circuit models and the nonstationary noise sources including 1/f noise, and the nonlinearity of the charge to voltage conversion.

There have been extensive study on noise in CMOS image sensors. During the whole procedure of design, fabrication, and characterization of CMOS image sensors, noise is always one of the most important parameters to be considered. This previous study helps us tremendously in understanding the noise problem in CMOS image sensors. However, in previous work it is often assumed that the circuit is time invariant, and that the noise sources are stationary. Stationary noise of a time invariant circuit can be readily analyzed in the frequency domain using spectral density functions.

In real image sensors the situation is quite different. The voltages, currents, conductances, and capacitances of the sensor circuitry are often changing rapidly. As a result, the noise is not stationary and the circuit is not time invariant. Under such conditions, the conventional frequency domain analysis often fails to generate results that are consistent with experiments.

Since MOSFETs are used inside each pixel, CMOS image sensors exhibit higher 1/f noise compared with CCD. This type of noise is particularly annoying to observers because of the low pass filtering characteristics of human eyes. The common technique for reducing 1/f noise is to increase the gate area of the transistor. However, in CMOS image sensors one must conserve as much chip area as possible for the photodetector. Even if the size can be increased, the use of a large area leads to an excessive input capacitance, which can adversely affect the charge conversion efficiency and bandwidth. The analysis of 1/f noise in a time varying circuit, again, is not well established.

In this thesis, we present the first complete and rigorous analysis of temporal noise

in CMOS image sensors that takes into consideration these complicating factors. We focus on developing the methodology and models. Since APS is the technology of choice for now and it well demonstrates the methods to analyze noise in CMOS image sensors, we will use it as the example sensor throughout this thesis. The methodology and models we developed here can be easily applied to analyze temporal noise in other image sensors, including both PPS and DPS.

1.3 Thesis Organization

Chapter 2 introduces the backgrounds for analyzing noise in CMOS image sensors. We first review the mathematical background for noise analysis, including random variables and random processes. We then go over the noise models of basic integrated circuit components, and introduce the superposition principle of finding the total output noise power for a linear circuit. We also describe the circuit, operation, and noise sources of CMOS photodiode APS, which we will use as an example throughout the thesis.

Chapter 3 presents a detailed and rigorous analysis of noise due to thermal and shot noise sources in photodiode APS. We show that during reset the conventional frequency domain noise analysis method cannot be applied. To calculate reset noise power we consider the time varying reset circuit model and perform time-domain noise analysis using the MOS transistor subthreshold noise model. We find that reset noise power is at most half of its commonly quoted $\frac{kT}{C}$ value, which corroborates the published experimental results. The lower reset noise, however, comes at the expense of image lag. We propose a new "pseudo-flash" reset method, which can alleviate image lag without increasing reset noise. We then present an analysis of photodiode shot noise that takes into consideration the nonlinearity of the photodiode charge to voltage conversion.

Chapter 4 describes the setup and methods we use to characterize CMOS APS. Using them we measure the capacitance, conversion gain, quantum efficiency, pattern noise, and temporal noise for the test structures fabricated in 0.35μ CMOS processes. We find that the measured reset noise mean square value is indeed close to $\frac{kT}{2C}$.

The measured SNR curve also matches well with our analysis. We demonstrate the incomplete reset induced image lag.

Chapter 5 proposes a nonstationary extension of the standard 1/f noise model, which accurately models 1/f noise when the transistor is switched from the off to the on state. We apply our nonstationary model to estimate the effect of 1/f noise on a periodically switched transistor, and a ring oscillator, respectively. In both cases we find that our estimates are consistent with the reported measurement results.

Chapter 6 presents the analysis of 1/f noise in CMOS APS. We analyze the 1/f noise due to the pixel level transistors using time domain analysis and our nonstationary 1/f noise model. We show that the conventional frequency domain analysis, which requires an arbitrarily defined low cutoff frequency, can produce very inaccurate estimates of 1/f noise power.

Finally chapter 7 concludes the thesis and discusses the most likely directions for future related research.

Chapter 2

Temporal Noise in CMOS Image Sensors

2.1 Introduction

Temporal noise is the temporal variation in pixel output values under constant illumination. Usually temporal noise in image sensors increases when the illumination gets stronger. At the same time the signal also increases, with a even faster speed. As a result the signal to noise ratio (SNR) usually improves as the illumination increases. Since it is SNR, instead of noise, that directly affects the image quality, the noise effect is most pronounced at low illumination levels. Noise also sets a fundamental limit on image sensor dynamic range (DR), which is another very important image quality metric.

There are many sources that can cause temporal noise in CMOS image sensors. Shot noise occurs when photo-electrons are generated and when dark current electrons are presented. Additional noise is added when resetting the photodetector (reset noise) and when reading out the pixel value (readout noise). If the output analog signal is to be digitized, then quantization noise must also be included. Power supply fluctuation can be coupled to the image sensor array and thus cause noise. Noise can also be injected to the sensor from peripheral circuits through substrate coupling. The environmental interferences such as temperature variation, light source humming,

electromagnetic field, *etc.*, can cause the fluctuation in the sensor output, and thus cause the temporal noise.

Some of the noise can be minimized by good circuit design practice. For example, substrate noise can be reduced by carefully implementing guard rings or by changing the layout. The power supply noise can be reduced by increasing the readout circuit power supply rejection ratio, or by simply using a cleaner power supply. Environmental interferences can be reduced by shielding, cabling, grounding, or by rearranging the whole setup. In the thesis, we are mainly concerned with the intrinsic noise that is generated internally by the CMOS image sensors. The intrinsic noise usually is hard to suppress, and is resulted from the physics of the integrated circuit devices. It includes three major types of noise, namely thermal noise, shot noise, and flicker noise.

In this chapter we go over some of the math and circuit background that is needed to analyze noise in CMOS image sensors. Then we describe the circuit and operation of CMOS active pixel sensors (APS), which we will be using as an example throughout the thesis.

The rest of the chapter is organized as follows. In section 2.2, we introduce the mathematical background for noise analysis, including random variables and random processes. In section 2.3 we describe the noise models of the basic integrated circuit components, and introduce the superposition principle of finding the total output noise power for a linear circuit. In section 2.4, we describe the circuit and operation of CMOS Active Pixel Sensors (APS). We then summarize the noise sources in CMOS APS.

2.2 Mathematical Background

Noise phenomena normally have the property that we do not specify precisely what magnitudes are observed at what time, either because we do not have the complete knowledge or because the precise description is not necessary. For this reason noise samples are conventionally modeled as continuously valued random variables, and noise waveforms are modeled as random processes. A continuous valued random

variable X is completely specified by its probability density function (pdf)

$$f_X(x) \geq 0, \quad \int_{-\infty}^{\infty} f_X(x)dx = 1. \tag{2.1}$$

From pdf one can calculate all the moments of the random variable. Among them the most important two for noise analysis are the mean

$$\overline{X} = \int_{-\infty}^{\infty} xf(x)dx,$$

and the mean square

$$\overline{X^2} = \int_{-\infty}^{\infty} x^2 f(x)dx.$$

Mean square is often interpreted as the average power of a signal X. Square root of this power (denoted as RMS) represents a equivalent constant signal with constant power equaling to the average power of X. From the mean and mean square, we can calculate the variance of X

$$\sigma_X^2 = \overline{X^2} - (\overline{X})^2,$$

which is interpreted as the square distance of X from its mean. When X has zero mean, its variance is equal to the mean square. Variance is often used to estimate the noise power.

The most often used random variable in noise analysis is Gaussian random variable. It is used to describe the magnitude distribution of a large variety of noise sources, including thermal, shot, and 1/f noise. Gaussian random variable has the well known "Bell Curve" pdf as depicted in Figure 2.1

$$f(x) = \frac{1}{\sqrt{2\pi\sigma_X^2}} e^{-\frac{(x-\overline{X})^2}{2\sigma_X^2}}. \tag{2.2}$$

In noise analysis, we also need to know the relationship between the noise sampled at different time points. This is conveniently modeled by a collection of multiple continuously valued random variables, which is completely specified by the joint probability distribution function. In the simplest case of two random variables X and Y,

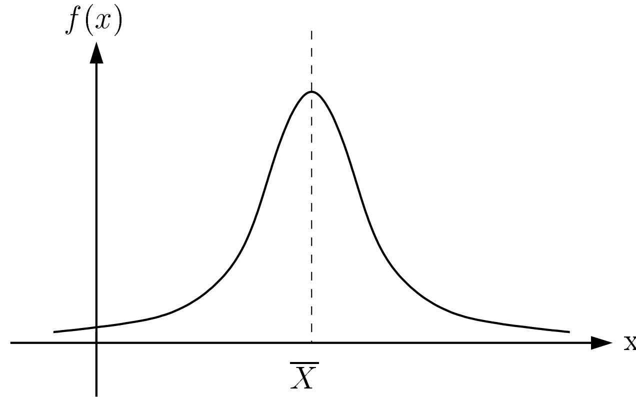

Figure 2.1: Probability density function of a Gaussian random variable.

the joint pdf f(x,y) must satisfy that

$$f(x,y) \geq 0, \quad \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} f(x,y)dxdy = 1. \tag{2.3}$$

The relationship between these two random variables X and Y is then described by the correlation function

$$\overline{XY} = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} xyf(x,y)dxdy. \tag{2.4}$$

If $\overline{XY} = \overline{X} \cdot \overline{Y}$, then X and Y are uncorrelated. If $f(x,y) = f_X(x)f_Y(y)$ they are independent of each other. It can be easily shown that two independent random variables must be uncorrelated. The reverse statement does not hold in general, although for jointly Gaussian random variables it is true.

A random process $X(t)$, $-\infty \leq t \leq \infty$ is used to model the noise waveform. It is an infinite collection of random variables (noise samples) indexed by time t. For any time instances $t_1, t_2, \ldots, t_n$, the samples $X(t_1), X(t_2), \ldots, X(t_n)$ are random variables. In noise analysis, it is often important to know the process mean $\overline{X}(t)$ and autocorrelation function $R_X(t+\tau, t) = \overline{X(t+\tau)X(t)}$.

Many important noise processes are modeled as stationary random processes, *i.e.*, processes with time invariant statistics. If both mean and autocorrelation function

are time invariant, i.e., $\overline{X}(t) = \mu$ and $R_X(t+\tau, t) = R_X(\tau)$, then $X(t)$ is a wide sense stationary (WSS) process and its autocorrelation function has the following properties

- $R_X(0) = \overline{X^2(t)}$, which has the interpretation of average process power.
- $R_X(\tau)$ is an even function.
- $|R_X(\tau)| \leq R_X(0)$, for all τ.

The power spectral density (psd) of a WSS process $X(t)$ is the Fourier Transform of $R_X(\tau)$

$$S_X(f) = \mathcal{F}[R_X(\tau)] = \int_{-\infty}^{\infty} R_X(\tau) e^{-j2\pi f\tau} d\tau, \quad -\infty \leq f \leq \infty \tag{2.5}$$

It can be shown that the psd must satisfy

- $S_X(f) \geq 0$, and is an even function.
- $P = \overline{X^2(t)} = \int_{-\infty}^{\infty} S_X(f) df$.
- $P[f1, f2] = 2\int_{f1}^{f2} S_X(f) df$,

where P denotes average power, and $P[f1, f2]$ denotes average power in frequency band $[f1, f2]$.

Of special importance to noise analysis is the band-limited white noise process. It is a WSS process, with zero mean $\overline{X}(t) = 0$, and a flat band-limited psd, as shown in Figure 2.2

$$S_X(f) = \begin{cases} \frac{P}{2}, & |f| < B \\ 0, & otherwise \end{cases} \tag{2.6}$$

So the autocorrelation function is

$$R_X(\tau) = PB\frac{\sin 2\pi B\tau}{2\pi B\tau} = PB\text{sinc}2B\tau, \tag{2.7}$$

which is depicted in Figure 2.3. In Figure 2.4 we plot an example waveform of a band-limited white noise process.

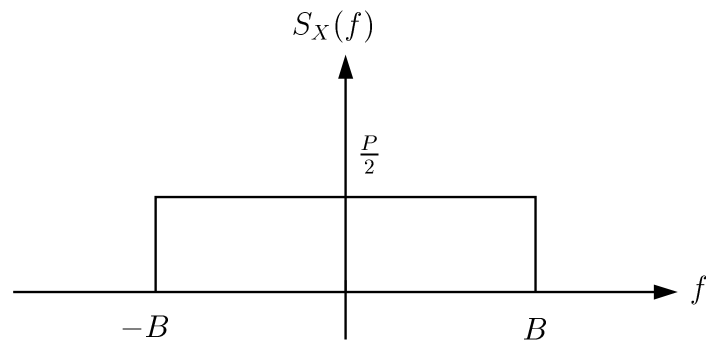

Figure 2.2: Power spectral density of a band-limited white noise process.

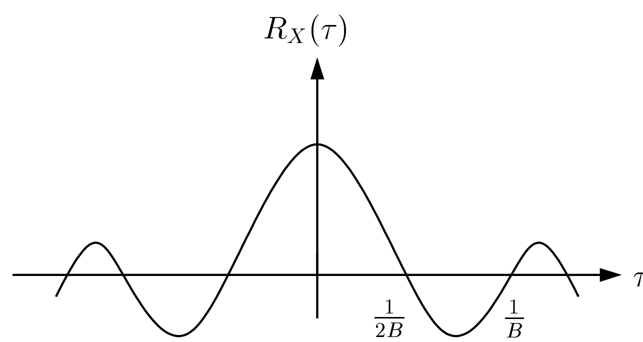

Figure 2.3: Autocorrelation function of a band-limited white noise process.

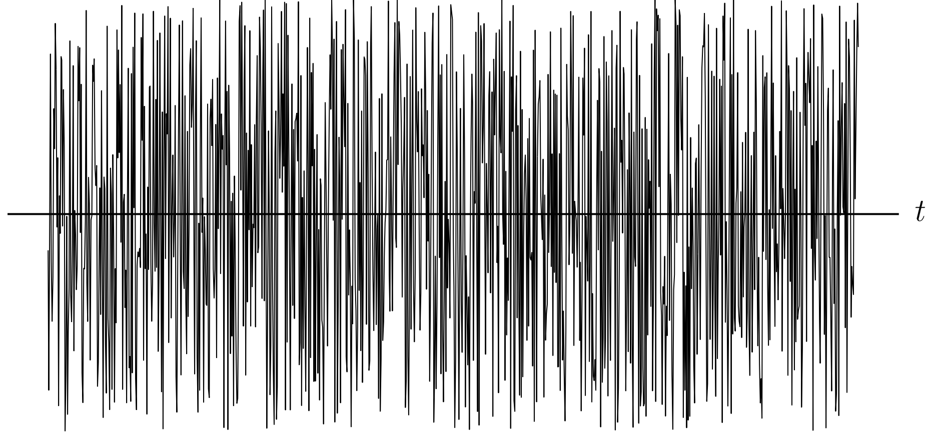

Figure 2.4: Waveform of a band-limited white noise process.

Now let $B \to \infty$, we get a white noise process. This is also WSS with

$$\begin{cases} \overline{X}(t) &= 0, \\ R_X(\tau) &= \frac{P}{2}\delta(\tau), \\ S_X(f) &= \frac{P}{2} \quad \forall f. \end{cases} \tag{2.8}$$

If $X(t)$ is a Gaussian random variable, then the white noise process is a white Gaussian noise (WGN). Two of the most important noise processes in integrated circuits, thermal and shot noise, are modeled as WGN processes.

In noise analysis it is often required to estimate the mean and the autocorrelation function of a stationary (and ergodic) noise process. There are two approaches to estimate them: the ensemble average and the time average. In the ensemble average approach, a large number of identical systems are constructed. They are measured simultaneously to extract the statistics we are interested. Although very powerful in theoretic noise analysis, this approach is not well suited for noise measurements. This is simply because a large number of identical systems are not available in practical experiments. Instead, the time average approach is often used to analyze experimental noise data, as far as the noise process is ergodic. In this time average approach, the mean is estimated by

$$< X(t) >_T = \frac{1}{T} \int_0^T X(T)dt, \tag{2.9}$$

and the autocorrelation is estimated by

$$< R_X(\tau) >_T = \frac{1}{T} \int_0^T X(T)X(T+\tau)dt. \tag{2.10}$$

Power spectral density is then found to be

$$S_X(f) = \frac{1}{n} \sum_{i=1}^{n} \mathcal{F}[< R_X(\tau) >_T^i]. \tag{2.11}$$

Note here that the psd cannot be estimated using the periodogram

$$\mathcal{F}[< R_X(\tau) >_T].$$

The estimator mentioned here estimates $R_X(\tau)$ n times and takes the average of the periodograms.

2.3 Noise in Integrated Circuits

In this section we introduce the physical models that are often used to analyze the noise in integrated circuits. We first describe the basic noise sources in integrated circuits. Then in subsection 2.3.2 we summarize the noise models of the most often used devices in CMOS image sensors, including the photodiode and the MOSFET. In subsection 2.3.3 we show how the noise contributions from different devices are summed together, to get the total output (or input) referred noise power.

2.3.1 Fundamental Noise Sources

There are many sources that can cause noise in today's integrated circuits, such as power supply fluctuation, EM interference, substrate coupling, *etc.* Often times these external interferences can be reduced to acceptable level, either by proper circuit design practice, or by carefully applying shielding and grounding techniques. In this

subsection we focus on the intrinsic noise that is hard to suppress, including thermal noise, shot noise, and flicker noise.

Thermal noise is generated by random thermally induced motion of electrons in resistive region, *e.g.*, carbon resistors, polysilicon resistors, MOS transistor channel in strong inversion. It is zero mean, and has a very flat and wide bandwidth (GHzs) Gaussian psd. Consequently it can be modeled as white Gaussian noise.

Thermal noise is represented either as a voltage source in series with a resistor R, as shown in the left part of Figure 2.5, with psd

$$S_V(f) = 2kTR, \quad \forall f \tag{2.12}$$

or equivalently as a current source in parallel with R with psd

$$S_I(f) = \frac{2kT}{R}, \quad \forall f \tag{2.13}$$

as shown in the right part of Figure 2.5.

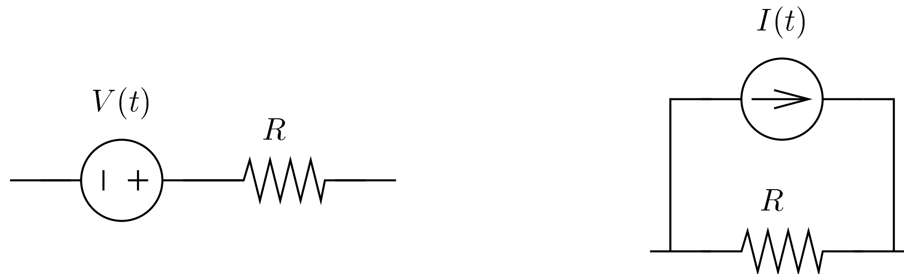

Figure 2.5: Noise model of a thermal noise source.

Shot noise is associated with the flow of current in diodes and bipolar transistors. It is generated by the fluctuations occurring when carriers cross a depletion region. There must be both a flow of current and a potential barrier to generate shot noise. Shot noise is also modeled as WGN, since it is zero mean, Gaussian and has a very flat and wide bandwidth psd. Shot noise is often represented by a

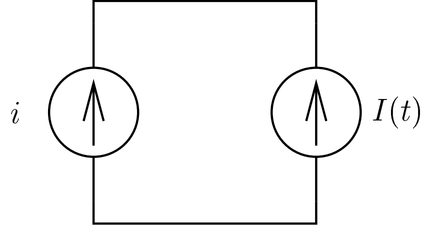

Figure 2.6: Noise model of a shot noise source.

current source in parallel with the dc source i as shown in Figure 2.6. Its psd is proportional to i

$$S_I(f) = qi, \quad \forall f \tag{2.14}$$

where q is the electron charge in Col.

Flicker noise is caused by traps due to crystal defects and contaminants in electronic devices. These traps randomly capture and release carriers, causing carrier number fluctuation. As a result, it is associated with dc current flow in both resistive and depletion regions.

Flicker noise has zero mean and psd that falls off with f

$$S_I(f) \propto i^c \frac{1}{|f|^n} \quad \text{for} \quad \frac{1}{2} \leq c \leq 2 \tag{2.15}$$

Often in semiconductor devices $n = 1$, and thus it is also called 1/f noise. The typical double sided 1/f noise psd is sketched in Figure 2.7

2.3.2 Noise Models for Photodiode and MOSFET

In this subsection we describe the noise models for the most commonly used semiconductor devices in CMOS image sensors, the photodiode and the MOSFET.

The dominant sources of noise in a photodiode are shot noise and 1/f noise due to the photocurrent and the dark current. In Figure 2.8 we plot the equivalent

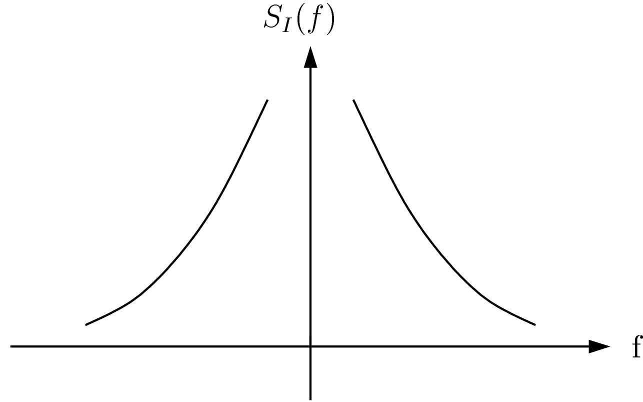

Figure 2.7: Power spectral density of 1/f noise.

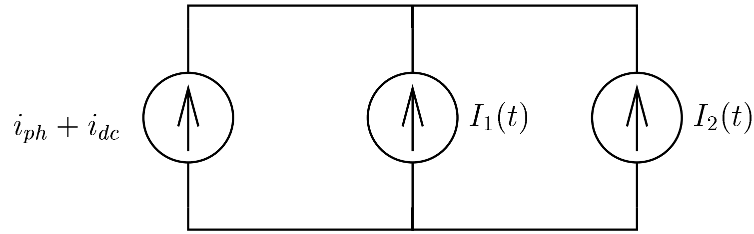

Figure 2.8: Noise Model of photodiode.

circuit model of a photodiode with two current sources representing shot and 1/f noise respectively.

The two current noise source have zero means and psds

$$S_{I_1}(f) = q(i_{ph} + i_{dc}) \quad \forall f \tag{2.16}$$

$$S_{I_2}(f) = a\frac{i_{dc}^c}{|f|} \quad \text{for } |f| \in [f_{min}, f_{max}], \tag{2.17}$$

where $0.5 \leq c \leq 2$ and a is a constant that depends on the physical characteristics of the diode.

Note that the two noise sources are statistically independent. Shot noise is caused by the electrons that randomly cross the depletion region. 1/f noise on the other

hand, is caused by the fluctuations in the surface recombination velocity and by the fluctuation in bulk carrier mobility. Thus it is often proportional to the density of surface states [27, 44, 52]. As a result, the 1/f noise is not simply related to the total current in the diode, but rather depends on the mechanism by which the current was generated. Typically the photodiodes in CMOS image sensors are reverse biased, where only dark current generates 1/f noise. By comparison, the shot noise is generated by the total current, including both dark current and photocurrent. In normal operation, the photocurrent should be much larger than the dark current, and thus 1/f noise in photodiode is much smaller than shot noise. Even if the currents causing shot and 1/f noise are the same, *i.e.*, under dark condition, 1/f noise is still less than shot noise unless the diode is operated at very low frequency, *e.g.*, below 1Hz.

Now we review the noise model for MOSFET, which is more complicated since it depends on the operating point of the transistor. In the traditional analog circuit design, MOS transistors are often biased into strong inversion regime. In this regime, the MOS transistor channel is resistive, and thus the dominant source of noise is thermal noise. Recently there are more and more circuit designs that use transistors biased in subthreshold regime. By doing so the designer can lower the power consumption, increase the circuit speed, or perform some analog signal processing. In the subthreshold regime, *i.e.*, for $0 < v_{gs} < v_T$, the dominant source of noise becomes shot noise. This is because in this regime the MOS transistor is operated in a way that is very similar to a bipolar transistor. In addition to the thermal or shot noise, MOS transistor also suffers from 1/f noise, which is mainly due to the traps in the gate oxide.

Noise in a MOS transistor is modeled by two statistically independent current sources, $I_1(t)$ for the thermal (or shot) noise and $I_2(t)$ for the flicker noise, in parallel with the drain current i_d, as shown in Figure 2.9

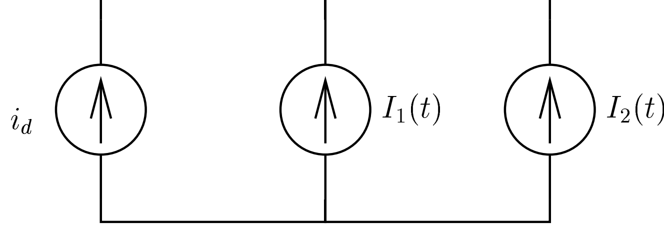

Figure 2.9: Noise Model of MOS transistor.

The thermal (or shot) noise source is modeled as a WGN with zero mean and psd

$$S_{I_1}(f) = \begin{cases} 2kT(\frac{2}{3}g_m) & \text{saturation} \\ \frac{2kT}{R} & \text{linear} \\ qi_d & \text{subthreshold,} \end{cases} \tag{2.18}$$

where g_m is the MOS transistor small signal transconductance, R is the transistor (source to drain) resistance in the linear region, and i_d is the drain current in subthreshold region.

The transconductance g_m can be further expressed as a function of bias voltages

$$g_m = \frac{\partial i_d}{\partial v_{gs}}\Big|_{\substack{v_{ds} = v_{ds0} \\ v_{gs} = v_{gs0}}} = \mu C_{ox}\frac{W}{L}(v_{gs0} - v_T)(1 + \lambda v_{ds0}), \tag{2.19}$$

where μ is the majority carrier mobility, C_{ox} is the gate capacitance density, v_{ds} is the drain source voltage, v_{gs} is the gate source voltage, v_T is the transistor threshold voltage, W and L are the transistor channel width and channel length, and λ is the channel length modulation coefficient.

Similarly, the resistance R is given by

$$R = \frac{\partial v_{ds}}{\partial i_d} \approx (\mu C_{ox}\frac{W}{L}(v_{gs0} - v_T))^{-1}, \tag{2.20}$$

provided that

$$v_{ds0} \ll (v_{gs0} - v_T).$$

The drain current in subthreshold is an exponential function of the bias voltages, and is given by

$$i_d = \frac{W}{L} i_0 e^{\frac{\kappa v_{gs} - (1-\kappa) v_{sb}}{v_t}} (1 - e^{-\frac{v_{ds}}{v_t}}), \tag{2.21}$$

where v_{gs} is the gate to source voltage, v_{ds} is the drain to source voltage, v_{sb} is the source to bulk voltage, κ is the gate efficiency factor, $v_t = \frac{kT}{q}$, and i_0 is a constant that depends on the transistor threshold voltage. Here κ can be computed from the gate capacitance and depletion capacitance

$$\kappa = \frac{C_{ox}}{C_{ox} + C_{depletion}}.$$

The flicker noise source $I_2(t)$ has zero mean and psd

$$S_{I_2}(f) = a \frac{i_d^c}{|f|} \text{ A}^2/\text{Hz}, \tag{2.22}$$

where a depends on the physical characteristics of the transistor. We will discuss flicker noise in detail in chapter 5.

2.3.3 Analysis of noise in linear circuits

In a practical circuit there usually exist multiple noise sources, and we are interested in finding the total noise power at a particular node, which is often either the output node or the input node. This requires the knowledge of transferring noise from its source to that particular node. Since noise is typically much smaller than signal, we can use linearized circuit models to analyze the effect of the different noise sources on the total noise power at that particular node.

In this section, we first describe how the linearized models can be used to analyze noise in linear circuits. We present two important examples that are often used in the analysis of noise in CMOS image sensors, the integrator circuit and the RC circuit. Then we discuss the noise analysis in linear circuits when multiple noise sources are

presented.

We shall see soon in the later part of the chapter that these methods are not sufficient to derive all the results we need to analyze noise in CMOS image sensors. Even if we use linear circuit models, in general the analysis can be complicated if the circuit is not in steady state, if the circuit parameters are time varying, or if the noise is not stationary. Furthermore, under some cases, the linear model itself has to be abandoned because the nonlinearity is pronounced.

We start with the integrator circuit as plotted in Figure 2.10. Assuming a zero mean WSS current source process $I(t)$ is applied to the integration capacitance at time $t = 0$, the output noise voltage for $t > 0$ is given by

$$V_o(t) = \frac{1}{C}\int_0^t I(\tau)d\tau. \tag{2.23}$$

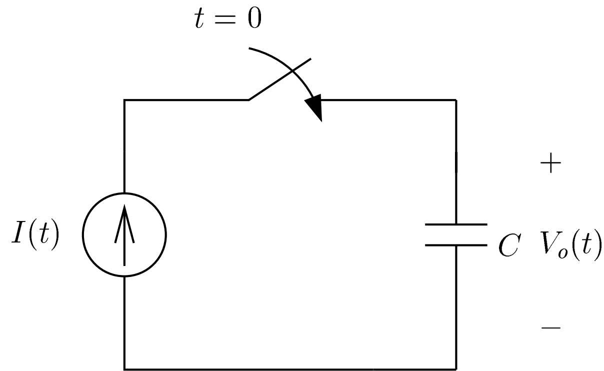

Figure 2.10: Integrator circuit.

Thus the mean is $\overline{V_o(t)} = 0$, and the average power is

$$\begin{aligned}
\overline{V_o^2(t)} &= \frac{1}{C^2}\int_0^t\int_0^t \overline{I(t_1)\cdot I(t_2)}dt_1dt_2 \\
&= \frac{1}{C^2}\int_0^t\int_0^t R_I(t_1-t_2)dt_1dt_2 \\
&= \frac{1}{C^2}\int_{-t}^t (t-|\tau|)R_I(\tau)d\tau,
\end{aligned}$$

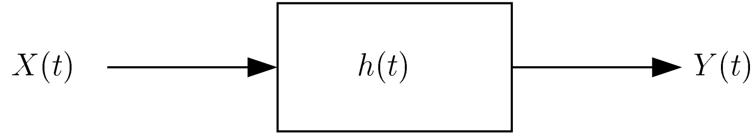

Figure 2.11: Linear time invariant circuit.

where $R_I(\tau)$ is the process autocorrelation function. If $I(t)$ is a white noise process with psd $\frac{P}{2}$, then $R_I(\tau) = \frac{P}{2}\delta(\tau)$ and

$$\overline{V_o^2(t)} = \frac{1}{C^2}\int_{-t}^{t}(t - |\tau|)\frac{P}{2}\delta(\tau)d\tau \quad (2.24)$$

$$= \frac{P}{2C^2}t \quad (2.25)$$

Now consider a linear time invariant circuit with impulse response $h(t)$ and input zero mean WSS voltage or current source process $X(t)$, as shown in Figure 2.11. In steady state, the output process $Y(t)$ is also WSS with zero mean and

$$S_Y(f) = |H(f)|^2 \cdot S_X(f), \quad (2.26)$$

where $H(f) = \mathcal{F}[h(t)]$ is the circuit transfer function.

Equation 2.26 is the basis of analyzing noise in linear time invariant circuits. The most often cited example using this equation is the RC circuit noise analysis, which results in the well known kT/C noise.

In Figure 2.12 we plot this simple RC circuit, where $V_i(t)$ is the thermal noise associated with R with psd $S_{V_i}(f) = 2kTR$. The transfer function of the circuit is given by

$$H(f) = \frac{1}{1 + j2\pi fRC}, \quad (2.27)$$

and thus

$$|H(f)|^2 = \frac{1}{1 + (2\pi fRC)^2}. \quad (2.28)$$

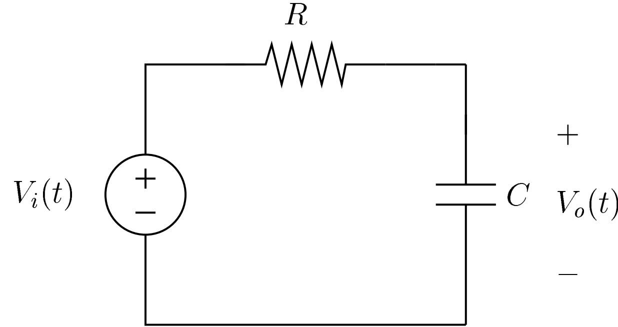

Figure 2.12: RC circuit.

So the output noise voltage psd is given by

$$S_{V_o}(f) = 2kTR\frac{1}{1+(2\pi fRC)^2}, \tag{2.29}$$

and the average output power is

$$\begin{aligned}\overline{V_o^2(t)} &= \int_{-\infty}^{\infty} S_{V_o}(f)df \\ &= \int_{-\infty}^{\infty} \frac{2kTRdf}{1+(2\pi fRC)^2} \\ &= \frac{2kTR}{2\pi RC}\arctan(x)|_{-\infty}^{\infty} \\ &= \frac{kT}{C}.\end{aligned}$$

Note that $\overline{V_o^2(t)} = \frac{kT}{C}$ is independent of R. This is because R is related to both the noise source psd and the circuit noise bandwidth. If R is increased, the noise source psd becomes higher, but the noise bandwidth becomes smaller in the same ratio. The two effects cancel each other and the total output noise power is kept unchanged.

Now consider a linear time invariant circuit with multiple zero mean, uncorrelated WSS noise sources $V_1(t), V_2(t), \ldots, V_k(t)$, as shown in Figure 2.13.

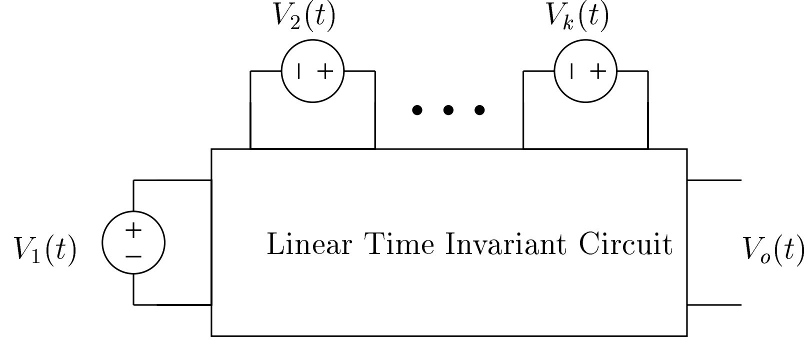

Figure 2.13: A linear time invariant circuit with multiple noise sources.

In steady state, the output noise voltage $V_o(t)$ is a zero mean WSS with psd

$$S_{V_o}(f) = \sum_{i=1}^{k} |H_i(f)|^2 S_{V_i}(f), \tag{2.30}$$

where $H_i(f)$ is the transfer function from the ith source to the output, and the average output power is given by

$$\overline{V_o^2(t)} = \int_{-\infty}^{\infty} S_{V_o}(f) df = \sum_{i=1}^{k} \overline{V_{oi}^2(t)}. \tag{2.31}$$

2.4 CMOS Photodiode Active Pixel Sensors

In real CMOS image sensors, the noise may not be stationary, the circuit may not be time invariant, and the circuit response may not be linear. To analyze noise under these complicated conditions, one cannot directly apply the methods we summarized in the previous sections. Instead, new methodology and models must be developed to accurately estimate the noise.

Throughout the thesis, we will be using CMOS photodiode APS as a particular example to demonstrate the development of these new methodology and models. So in this section we first provide an overview of the CMOS photodiode APS circuit and operation, and then describe the noise sources in this circuit.

The photodiode APS circuit we analyze in this thesis is a typical 3 transistor photodiode APS, as shown in Figure 2.14. The circuit can be divided into 3 levels: pixel level, column level, and chip level. Each pixel circuit contains in addition to a photodiode, a reset transistor M1, a source follower transistor M2, and an access transistor M3. The pixel circuit is duplicated to form the sensor array. Column circuit includes a bias transistor M4, which acts as the current source of the pixel source follower amplifier, a storage capacitor C_o, and some other column amplifier and signal conditioning circuits. Column circuit is duplicated to form a row placed at the bottom of the chip. Chip level circuit can be as simple as a buffer that drives the output pad.

There are two signals connected to each pixel: signal Word and signal Reset. Their states separate the sensor's operation into 3 steps: reset, integration, and readout. The sensor operation is illustrated by the timing diagram at the bottom part of Figure 2.14. As can be seen, the sensor is reset, and read out one row at a time. At the end of each row's integration time, the pixel values are read out and stored onto the column storage capacitors C_{oj}. The whole row is then reset and the stored pixel values are transferred to the output amplifier via the column multiplexer. Correlated double sampling, which is typically performed to reduce fixed pattern noise (FPN), is not shown in the timing diagram. Its effect on temporal noise can be readily analyzed using the results derived in the thesis.

We are interested in finding the input referred RMS noise value at node IN in volts. To compute it, we sum up the output referred noise power generated during each step of the APS operation, *i.e.*, reset, integration, and readout, and then transfer it back to input node using the circuit transfer function. Noise generated during readout is directly computed at the output node. Noise generated during reset and integration are sampled onto C_o first, and then transferred to the output during readout.

In analyzing noise generated during each step of the sensor operation, we will pay special attention to the pixel level circuit. This is because in a typical CMOS photodiode APS, pixel level circuit generates most of the noise. It is also because the noise analysis of pixel level circuit best demonstrates the necessity of developing new models and methodology. As we shall see in later chapters, the transistors of the

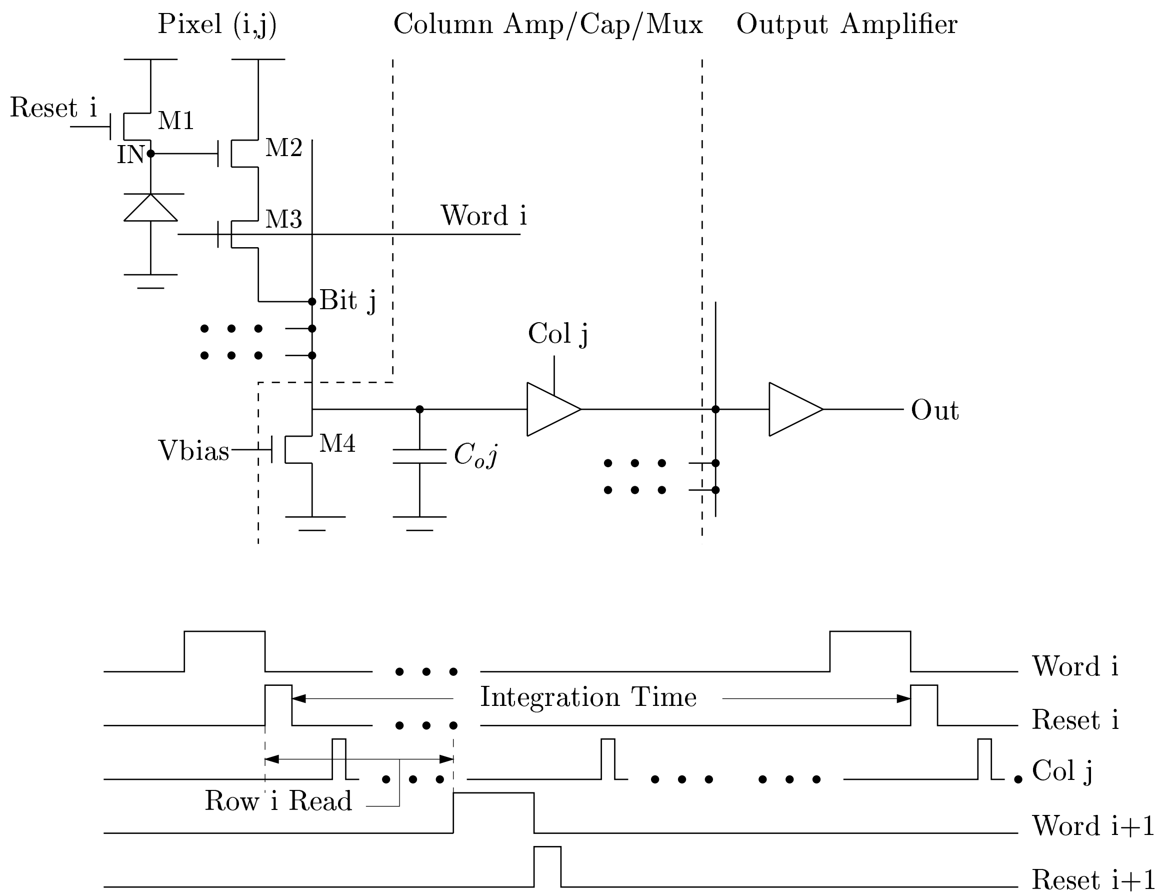

Figure 2.14: CMOS photodiode APS circuit and timing diagram.

	Steady state circuit model	Non-steady state circuit model
Stationary noise	Follower (thermal) Access (thermal)	Photodiode (shot)
Nonstationary noise	Follower (1/f) Access (1/f)	Reset (shot, 1/f)

Figure 2.15: Noise sources in CMOS APS pixel level circuit.

pixel level circuit work at almost every possible regime, including saturation, linear, and subthreshold. They also cover all the combinations of steady/nonsteady state circuit and stationary/nonstationary noise sources. Even worse, the pixel circuit is quite nonlinear during the integration time.

Figure 2.15 summarizes the noise sources presented in a typical CMOS APS pixel level circuit. As can be seen, the analysis of shot and 1/f noise due to the reset transistor is particularly complicated, involving both a nonsteady state circuit model (actually time varying) and a nonstationary noise source. By comparison, the thermal noise due to the follower and the access transistor can be accurately estimated using the stationary noise sources and steady state circuit models. This is the only combination in the figure that has been accurately analyzed by the conventional frequency domain noise analysis methods. In the thesis, we will develop methods to better estimate noise effects for all other 3 combinations.

In the following chapters, we will analyze thermal noise and shot noise, using time domain noise analysis method to deal with the time varying circuits. Analysis of 1/f noise then follows. Since the current 1/f noise models are not sufficient to handle switched circuits, we will start from the basic theorem to derive a nonstationary 1/f noise model first, and then use it to analyze 1/f noise in CMOS APS.

2.5 Summary

We reviewed the basic math background that is necessary for noise analysis, including random variables and random processes. We then go over the often used circuit noise analysis models and methods, such as the noise models for fundamental noise sources in integrated circuits, the noise models for basic semiconductor devices in CMOS image sensors, and the methods to analyze noise in a linear circuit. CMOS photodiode APS circuit is then presented together with its operation and noise sources. We note that the pixel level circuit generates most of the noise, and involves all combinations of steady/nonsteady state circuit models and stationary/nonstationary noise sources. It is a good example to demonstrate the necessity of developing new models and methodology to analyze noise in CMOS image sensors, and will be used throughout the thesis.

Chapter 3

Analysis of Thermal and Shot Noise in CMOS APS

3.1 Introduction

Hand analysis of thermal and shot noise in CCDs and CMOS APS have been published by several authors [49, 19, 23, 3, 56, 34, 5]. Their analysis shows that at low illumination the dominant source of noise is reset and readout transistors thermal and shot noise, while at high illumination the dominant source of noise is the photodiode shot noise. The noise power due to the reset transistor, which is sampled at the end of reset, is often quoted to be $\frac{kT}{C}\mathrm{V}^2$. Recent experiments [57, 45], however, showed that the measured reset noise is significantly smaller than $\frac{kT}{C}$. In analyzing noise due to photodiode shot noise it is often assumed that the photodiode charge to voltage relation is linear. As supply voltage scales with CMOS technology this relation is becoming increasingly nonlinear.

In this chapter we present a detailed and rigorous analysis of noise due to thermal and shot noise sources in photodiode APS that takes into consideration these complicating factors. We show that during reset the reset transistor operates in subthreshold and steady state is not achieved. As a result, the conventional frequency domain noise analysis method cannot be applied. To calculate reset noise power we consider the time varying reset circuit model and perform *time-domain* noise analysis

using the MOS transistor subthreshold noise model [53]. We show that reset noise power is at most half of its commonly quoted $\frac{kT}{C}$ value, which corroborates the published experimental results. The lower reset noise, however, comes at the expense of image lag. Since steady state is not reached during reset, the final photodiode reset voltage depends on its initial value. This problem can be alleviated by overdriving the gate of the reset transistor or by using a pMOS instead of an nMOS transistor for reset. These techniques, however, double the reset noise power. We propose a new "pseudo-flash" reset method, which can alleviate image lag without increasing reset noise. We then present an analysis of photodiode shot noise that takes into consideration the nonlinearity of the photodiode charge to voltage conversion. We again perform time-domain noise analysis using a time varying circuit model. We find that the nonlinearity actually improves SNR at high illumination.

The rest of the chapter is organized as follows. In section 3.2 we present our analysis of reset noise using time domain analysis. In section 3.3 we discuss the image lag due to incomplete reset and present our pseudo-flash reset method. In section 3.4 we present the analysis of the photodiode shot noise that takes into consideration the nonlinearity of the photodiode charge to voltage conversion. In section 3.5 we use SPICE to estimate the noise contributions of the follower, access and column amplifier transistors. We find that the contributions of these transistors to the noise is negligible compared to reset and photodiode shot noise.

3.2 Noise Due to Reset

During reset the gate of the reset transistor M1 is set to a high voltage, typically v_{dd}. At the beginning of reset, M1 is either operating in the saturation region or in subthreshold depending on the photodiode voltage at the end of integration. If the photodiode voltage is low enough, M1 is in saturation at first and for a very short amount of time before it goes into subthreshold for the rest of reset. Note that this source follower reset circuit configuration and operation is widely used also in CCD image sensors to implement the output stage reset.

The circuit noise model during reset is shown in Figure 3.1. The current source

$I_d(t)$ models the transistor shot noise, while the current source $I_s(t)$ models the shot noise due to photodiode dark current i_{dc} and photocurrent i_{ph}. In subthreshold, $I_d(t)$ can be modeled as a white Gaussian noise process with the two sided power spectral density (psd) [53]

$$S_{I_d}(f) = qi_d \text{ A}^2/\text{Hz}, \tag{3.1}$$

where i_d is the drain current of M1. The photodiode noise source $I_s(t)$ is also mainly due to shot noise and has the psd

$$S_{I_s}(f) = q(i_{ph} + i_{dc}) \text{ A}^2/\text{Hz}. \tag{3.2}$$

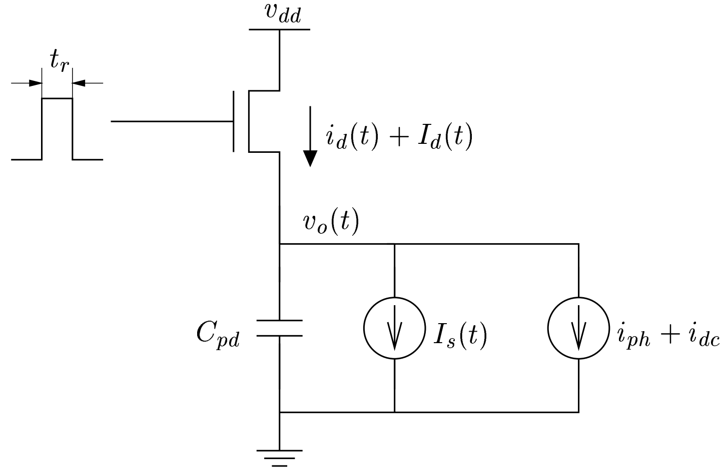

Figure 3.1: CMOS APS circuit noise model during reset.

If the reset time t_r is sufficiently greater than the settling time t_{settle}, *i.e.*, the time at which the transistor subthreshold current i_d equals the photodiode current $i_{ph} + i_{dc}$, then steady state is achieved and the average reset noise power is given by

$$\overline{V_n^2} = \int_{-\infty}^{\infty} \frac{2q(i_{ph} + i_{dc})}{(g_{m1} + g_{mb1})^2} \frac{1}{1 + (2\pi f \frac{C_{pd}}{(g_{m1}+g_{mb1})})^2} df, \tag{3.3}$$

where g_{m1} and g_{mb1} are the transconductances of M1 in subthreshold, and the factor

of 2 is due to the fact that in steady state $i_d = i_{ph} + i_{dc}$. Performing the integral we get that

$$\overline{V_n^2} = \frac{q(i_{ph} + i_{dc})}{C_{pd}(g_{m1} + g_{mb1})}. \tag{3.4}$$

Since in subthreshold $i_d = \frac{kT}{q}(g_{m1} + g_{mb1})$, we get $\overline{V_n^2} = \frac{kT}{C_{pd}}$, which is the same as the often quoted reset noise value.

This analysis, however, holds only if steady state is achieved during reset, which can only occur if the settling time is shorter than the reset time. To find out whether the circuit is in steady state, we need compute the settling time t_{settle}. Applying Kirchhoff's current law we get that

$$\frac{dV_{pd}(t)}{dt} = \frac{i_d(t) + I_n(t) - i_{ph} - i_{dc}}{C_{pd}(V_{pd}(t))}, \tag{3.5}$$

where $I_n(t) = I_d(t) + I_s(t)$ and V_{pd} is the photodiode voltage. Assuming that the signal is much larger than the noise, which is true for the circuit we analyze, we can express the photodiode voltage during reset as the sum of a signal voltage $v_{pd}(t)$ and a noise voltage $V_n(t)$, *i.e.*, $V_{pd}(t) = v_{pd}(t) + V_n(t)$, and approximate the capacitance $C_{pd}(V_{pd}(t)) \approx C_{pd}(v_{pd}(t)) + \frac{dC_{pd}}{dv_{pd}} V_n(t)$. With these approximations, we can write the signal part of equation 3.5 as

$$\frac{dv_{pd}(t)}{dt} = -\frac{i_{ph} + i_{dc}}{C_{pd}(v_{pd}(t))} + \frac{i_d(v_{pd}(t))}{C_{pd}(v_{pd}(t))}. \tag{3.6}$$

To calculate settling time using this equation, we need first find the time t_1 at which the reset transistor transitions from above to below threshold. The reset transistor then operates in subthreshold for a period of $t_2 = t_{settle} - t_1$ until it reaches steady state, *i.e.*, until its drain current almost equals $i_{ph} + i_{dc}$.

While the reset transistor is operating above threshold, its drain current is given by [35]

$$i_d(t) = \frac{W}{2L} C_{ox} \mu_n (v_{dd} - v_{th}(v_{pd}) - v_{pd})^2, \tag{3.7}$$

where W and L are the transistor channel width and length, C_{ox} is the gate oxide capacitance (per unit area), μ_n is the electron mobility, and v_{th} is the threshold

voltage.

Note here v_{th} is also a function of v_{pd}

$$v_{th}(v_{pd}) = v_{th0} + \gamma(\sqrt{v_{pd} + 2|\phi_p|} - \sqrt{2|\phi_p|}) \ \ \mathrm{V}, \tag{3.8}$$

where v_{th0} is the threshold voltage at 0V source-substrate bias, γ is the body effect parameter, and ϕ_p is the bulk potential.

For most of the reset time M1 operates in subthreshold, and i_d can be expressed as [31]

$$i_d(t) = \frac{W}{L} I_0 e^{\left[\frac{(v_g - v_{pd})\kappa}{v_T} - \frac{(v_{pd} - v_b)(1-\kappa)}{v_T}\right]}(1 - e^{-\frac{(v_d - v_{pd})}{v_T}}), \tag{3.9}$$

where v_g is the gate voltage, v_d is the drain voltage, v_{pd} is the source voltage, v_b is the bulk voltage, κ is the gate efficiency factor, $v_T = \frac{kT}{q}$, and I_0 is a constant that depends on the transistor threshold voltage.

The transition between above and below threshold occurs when the currents calculated using equations 3.7 and 3.9 are equal. Assuming the circuit parameters of the test structure which will be described in chapter 4, we find that the transition voltage v_1, *i.e.*, the voltage at which this transition occurs, $\approx$ 2V. The transition time t_1 is $\leq$ 0.2ns even when the photodiode voltage $v_{pd}(0)$ is very low.

To find t_2, we first set $v_1 = 2\mathrm{V}$ and assume that the capacitance $C_{pd}(v_{pd}(t)) = C_{pd}$, *i.e.*, is independent of t. Defining $K_0 = \frac{W}{L} I_0 e^{\frac{v_g \kappa}{v_T}}$ and substituting from equation 3.9 into equation 3.6 then solving it, we get that

$$v_{pd}(t) = v_T \ln \frac{-K_0 + K_0 e^{\frac{i_c t}{v_T C_{pd}}} + i_c e^{\frac{v_1}{v_T}}}{i_c e^{\frac{i_c t}{v_T C_{pd}}}}, \tag{3.10}$$

where $i_c = i_{ph} + i_{dc}$, and the time origin is shifted such that $t = 0$ corresponds to the time when the reset transistor enters subthreshold.

Combining equations 3.10 and 3.9 we can explicitly write $i_d(t)$ as a function of time. Now assuming that steady state is achieved for $i_d(t) \approx i_c$ we find that

$$t_2 = \frac{v_T C_{pd}}{i_c} \ln \frac{K_0}{i_c e^{\frac{v_1}{v_T}} - K_0}. \tag{3.11}$$

Thus we get the settling time $t_{settle} = t_1 + t_2$, which is more than 1ms for typical illumination conditions.

Figure 3.2 plots the settling time as a function of photocurrents, which shows that $t_{settle} \geq 1$ms even for very high photocurrents. This settling time is much larger than the typical reset time, which is typically in the few microseconds range. Therefore steady state is not achieved during reset and we must analyze the reset noise for a time varying circuit model using time domain analysis.

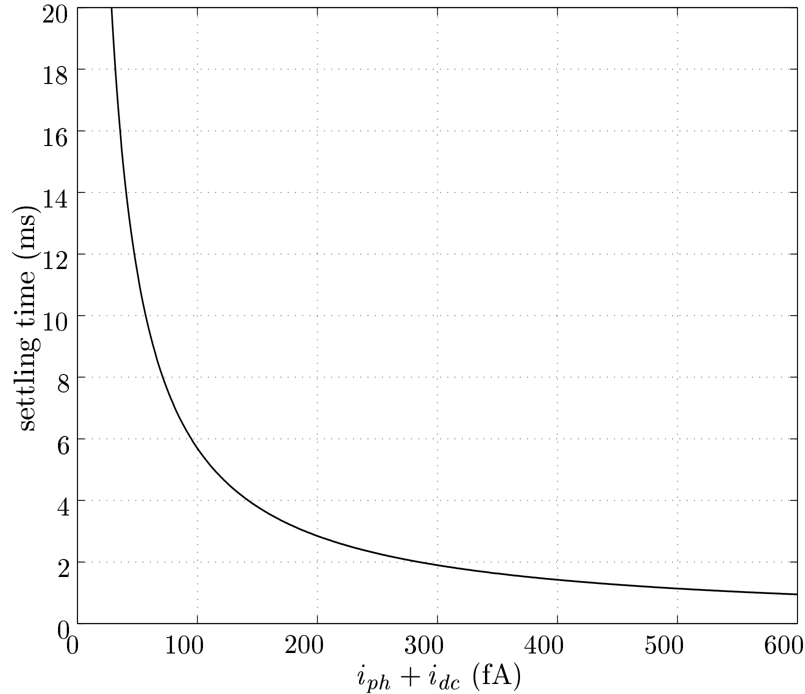

Figure 3.2: Reset settling time t_{settle} vs. photodiode current.

To perform this time domain analysis, first note that i_d is a function of $(v_{pd}(t) + V_n(t))$. Linearizing around the signal voltage $v_{pd}(t)$ we get that $i_d(t) \approx i_d(v_{pd}(t)) - g(t)V_n(t)$, where $g(t) = -\frac{di_d}{dv_{pd}}$ is the total transistor transconductance. Also note that during reset the photodiode capacitance changes very little, and thus we can write

$C_{pd}(V_{pd}(t)) \approx C_{pd}(v_{pd}(t))$. The noise part of equation 3.5 is thus given by

$$I_n(t) = C_{pd}(v_{pd}(t))\frac{dV_n(t)}{dt} + g(t)V_n(t). \tag{3.12}$$

Note that this is a general first order linear differential equation and the solution at the end of reset can be expressed as a functional of the noise source current

$$V_n(t_r) = \int_0^{t_r} \frac{I_n(\tau)}{C_{pd}(\tau)} e^{-\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}(\tau_0)} d\tau_0} d\tau. \tag{3.13}$$

When the noise autocorrelation function is a δ function, which is the case for thermal and shot noise we get that

$$\overline{V_n^2(t_r)} = \int_0^{t_r} \frac{R(\tau)}{C_{pd}^2(\tau)} e^{-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}(\tau_0)} d\tau_0} d\tau, \tag{3.14}$$

where $R(\tau)$ is the psd of the (white) noise source. For a more general noise process, a similar formula was derived in [50].

It can be readily verified from equation 3.14 that the contribution from the noise above threshold is extremely small, and can thus be ignored. We can also ignore the shot noise associated with $i_{ph} + i_{dc}$, since these currents are much smaller than the reset transistor drain current. With these simplifying assumptions, $R(\tau) = qi_d(\tau)$, and $C_{pd}(\tau)$ is a constant, which we denote by C_{pd}.

To find $\overline{V_n^2(t_r)}$, we need to evaluate the inner integral in equation 3.14. To calculate $g(t)$, we need to calculate the signal voltage $v_{pd}(t)$ first. Given that $i_{ph} + i_{dc} << i_d(t)$, we can approximate equation 3.10 by

$$v_{pd}(t) \approx v_T \ln(\frac{K_0 t}{v_T C_{pd}} + e^{\frac{v_1}{v_T}}), \tag{3.15}$$

where $v_T = \frac{kT}{q}$, $K_0 = \frac{W}{L} I_0 e^{\frac{v_g \kappa}{v_T}}$, v_1 is the transition voltage, and $t = 0$ corresponds to the time when the reset transistor enters subthreshold. We let $\delta = \frac{v_T C_{pd}}{i_d(0)}$ be the *thermal time*, *i.e.*, the time to charge the photodiode capacitance to v_T using $i_d(0)$. Substituting in the I–V characteristics of the MOS transistor in subthreshold, we get

that

$$i_d(\tau) \approx \frac{v_T C_{pd}}{\tau + \delta}. \tag{3.16}$$

Now evaluating the inner integral in equation 3.14 with $t_r - t_1$ replacing t_r, and $g(t) = \frac{i_d(t)}{v_T}$ we get that

$$\int_{\tau}^{t_r - t_1} \frac{g(\tau_0)}{C_{pd}(\tau_0)} d\tau_0 = \int_{\tau}^{t_r - t_1} \frac{1}{\tau_0 + \delta} d\tau_0 = \ln \frac{t_r - t_1 + \delta}{\tau + \delta}. \tag{3.17}$$

Substituting into equation 3.14, we get the mean square noise voltage at the end of reset

$$\overline{V_n^2(t_r)} = \frac{1}{2}\frac{kT}{C_{pd}}(1 - \frac{\delta^2}{(t_r - t_1 + \delta)^2}). \tag{3.18}$$

Thus the mean square reset noise voltage is less than $\frac{1}{2}$ of the often quoted $\frac{kT}{C_{pd}}$ value. Since t_r is typically in the few microsecond range, while $t_1 \leq 0.2$ns and $\delta \approx 6$ns for our test structure circuit, the mean square reset noise voltage value is in fact very close to $\frac{kT}{2C_{pd}}$. For example assuming $C_{pd} = 22$fF, which is consistent with the circuit in our test structure discussed in section 4.3, we get an input referred RMS reset noise voltage of 303μV at room temperature.

The intuitive reason for the $\frac{kT}{2C_{pd}}$ result is twofold. First, by inspecting equation 3.14 we see that the noise decays exponentially while it is being integrated onto C_{pd}. In subthreshold where the transistor I–V relation is exponential, the decay and integration balance each other and the the circuit is in "virtual" steady state. The second reason is that in the case we are considering, shot noise due to the reset transistor drain current dominates, which in steady state contributes only $\frac{kT}{2C_{pd}}$ [42].

If reset time is long enough steady state is eventually reached. In this case, the noise power should become $\frac{kT}{C_{pd}}$ as calculated using conventional frequency domain analysis. Now we show that time domain analysis gives the same result.

When steady state is reached, the noise due to the photodiode photo and dark currents can no longer be ignored. To simplify notation we define $i_d' = i_{ph} + i_{dc}$. The autocorrelation function of the shot noise due to both the reset transistor and the

photodiode is thus given by

$$R(t) = \begin{cases} qi_d(t) + qi'_d & t < t_{settle} \\ 2qi'_d, & t \geq t_{settle}. \end{cases} \tag{3.19}$$

Now define $g' = \frac{qi'_d}{kT}$, then for $t \geq t_{settle}$ $g(t) = g'$. Using equation 3.14 we get the mean square noise voltage

$$\begin{aligned}
\overline{V_n^2(t_r)} &= \int_0^{t_{settle}} \frac{qi_d(\tau) + qi'_d}{C_{pd}^2} e^{-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}} d\tau_0} d\tau + \int_{t_{settle}}^{t_r} \frac{2qi'_d}{C_{pd}^2} e^{-2\int_\tau^{t_r} \frac{g'}{C_{pd}} d\tau_0} d\tau \\
&= \int_0^{t_{set}} \frac{qi_d(\tau)}{C_{pd}^2} e^{-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}} d\tau_0} d\tau + \int_0^{t_{set}} \frac{qi'_d}{C_{pd}^2} e^{-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{pd}} d\tau_0} d\tau \\
&\quad + \int_{t_{set}}^{t_r} \frac{2qi'_d}{C_{pd}^2} e^{-2\int_\tau^{t_r} \frac{g'}{C_{pd}} d\tau_0} d\tau \\
&= \int_0^{t_{settle}} \frac{qi_d(\tau)}{C_{pd}^2} e^{-2\int_\tau^{t_{settle}} \frac{g(\tau_0)}{C_{pd}} d\tau_0} d\tau \; e^{-2\int_{t_{settle}}^{t_r} \frac{g'}{C_{pd}} d\tau_0} \\
&\quad + \frac{qi'_d}{C_{pd}^2} \int_0^{t_{settle}} \frac{(\tau + \delta)^2}{(t_{settle} - t_1 + \delta)^2} d\tau \; e^{-2\int_{t_{settle}}^{t_r} \frac{g'}{C_{pd}} d\tau_0} \\
&\quad + \frac{2qi'_d}{C_{pd}^2} \int_{t_{settle}}^{t_r} e^{-2\frac{g'}{C_{pd}}(t_r - \tau)} d\tau.
\end{aligned} \tag{3.20}$$

Using the same method that we derived equation 3.18, equation 3.20 can be simplified into

$$\begin{aligned}
\overline{V_n^2(t_r)} &= \frac{1}{2}\frac{kT}{C_{pd}}(1 - \frac{\delta^2}{(t_{settle} - t_1 + \delta)^2}) \; e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})} \\
&\quad + \frac{1}{3}\frac{qi'_d}{C_{pd}^2}((t_{settle} - t_1 + \delta) - \frac{\delta^3}{(t_{settle} - t_1 + \delta)^2}) \; e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})} \\
&\quad + \frac{kT}{C_{pd}}(1 - e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})}) \qquad (3.21) \\
&\approx \frac{1}{2}\frac{kT}{C_{pd}} \; e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})} + \frac{1}{3}\frac{qi'_d t_{settle}}{C_{pd}^2} \; e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})} \\
&\quad + \frac{kT}{C_{pd}}(1 - e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})}).
\end{aligned}$$

The first term of the above equation is due to the reset transistor shot noise during the non-steady state period. Similarly, the second term is due to the photodiode shot noise noise during the non-steady state period. Using $i'_d = i_d(t_{settle}) \approx \frac{v_T C_{pd}}{t_{settle}+\delta}$ (equation 3.16), we get that $\frac{1}{3}\frac{q i'_d t_{settle}}{C_{pd}^2} \approx \frac{1}{3}\frac{kT}{C_{pd}}$. As expected the second term is smaller than the first, since for $t < t_{settle}$ $i'_d < i_d(t)$. The last term represents the noise generated during $t \geq t_{settle}$.

As $t_r \to \infty$, $e^{-2\frac{g'}{C_{pd}}(t_r - t_{settle})}$ approaches zero and the first two terms vanish. This confirms that the noise generated before t_{settle} finally decays to zero. The last term on the other hand approaches $\frac{kT}{C_{pd}}$, which is the same as the steady state result obtained using frequency domain analysis.

We now verify that the above derivation also leads to $\frac{kT}{2C_{pd}}$ for $t \ll t_{settle}$. It is clear that in this case the third term of equation 3.21 does not exist. The second term can be ignored, since $i'_d \ll i_d(t_r)$, $\frac{1}{3}\frac{q i'_d t_r}{C_{pd}^2} \ll \frac{1}{3}\frac{kT}{C_{pd}}$. This leaves us with the first term which is equal to the right-hand side of equation 3.18.

3.3 Image Lag Due to Incomplete Reset

In the previous section we found that reset noise power is at most half of its commonly quoted $\frac{kT}{C}$ value. This reduction in noise, however, comes at the expense of image lag. Since steady state is not reached, the final reset voltage can depend on the photodiode voltage at the beginning of reset, and thus resulting in image lag. Note that the source of image lag here is different from the source of image lag in CCDs, where image lag is caused by incomplete charge transfer and can be eliminated using a pinned photodiode [48]. In this section, we explore the image lag problem in CMOS APS, and propose a new reset method, which alleviates lag without increasing reset noise.

To analyze image lag we assume the standard APS circuit and operation described in section 2.4. In Figure 3.3, we plot the simulated photodiode voltage waveform for four different frame to frame illumination conditions assuming integration time $t_{int} =$ 30ms, reset time $t_r = 1\mu$s, dark current $i_{dc} = 2.3$fA, and bright level photocurrent $i_{ph} = 50$fA. The *bright* condition in the figure refers to the case where the photodiode

voltage at the end of integration is low enough so that at the beginning of the next reset, the reset transistor operates above threshold.

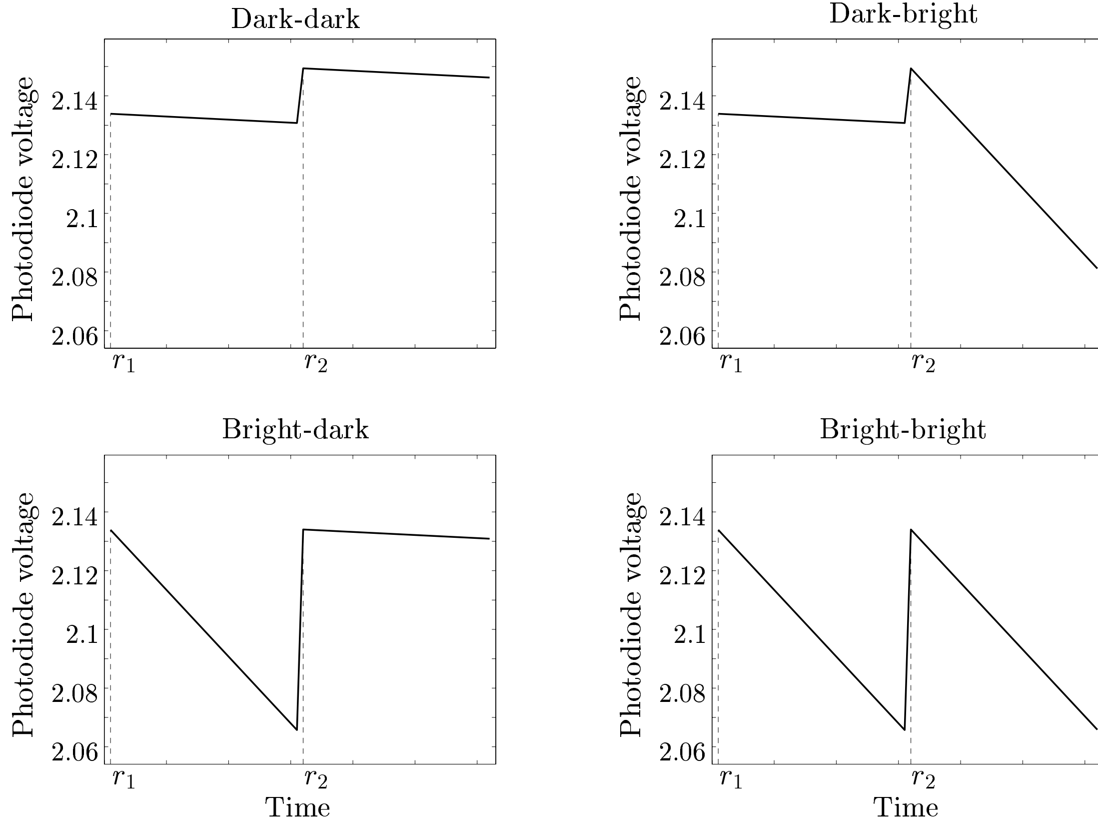

Figure 3.3: Simulated photodiode voltage waveform due to incomplete reset. r_1 and r_2 refer to the end of reset for the first and second frames respectively.

As can be seen, if the first frame is bright, then the final reset voltages for the two frames are the same. On the other hand, if the first frame is dark, the final reset voltage for the second frame is noticeably different from that of the first frame, resulting in image lag. To see why, note that at the beginning of reset, following a bright frame, the reset transistor operates above threshold (for ≤ 0.2ns). Therefore it reaches the transition voltage v_1 very quickly and spends almost all of the reset time in subthreshold. Thus, the final reset voltage is virtually independent of the initial photodiode voltage. For example, assuming a 1μs reset time, the final reset voltage

can only vary by at most 5μV as a function of the brightness of the previous frame, which is much smaller than the reset noise.

Reset induced image lag can be eliminated using a pMOS reset transistor or by overdriving the reset transistor gate as shown in Figure 3.4. In both cases the reset transistor operates in the linear region during reset. Thus the final reset voltage is v_{dd}, independent of the initial photodiode voltage, and lag is eliminated. However, reset noise is significantly increased. First the noise due to the reset transistor is increased to $\frac{kT}{C_{pd}}$. Secondly, noise may be introduced due to the resistive coupling to the supply voltage [45]. Using pMOS transistor also has the disadvantage of increased pixel area.

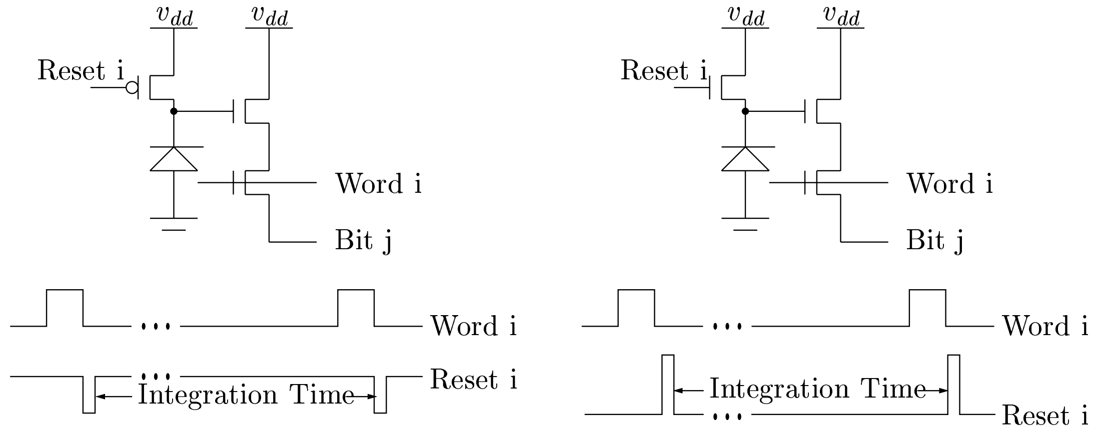

Figure 3.4: pMOS (left) and overdriving gate (right) reset methods.

To achieve both low reset noise and low lag, we propose the new reset method shown in Figure 3.5. The reset transistor drain is connected to a signal called Reset_dr instead of directly to the supply voltage v_{dd}. As shown in the figure Reset_dr is dropped to a low voltage, *e.g.*, ground, at the beginning of reset. This "pseudo-flash" operation ensures that the reset transistor always starts above threshold, thus eliminating lag. At the same time reset noise is not increased and is still equal to $\frac{kT}{2C_{pd}}$.

Reset_dr
v_{dd}
Reset i
Word i
Bit j
Word i
Integration Time
Reset i
Reset_dr

Figure 3.5: Pseudo-flash reset method.

3.4 Noise Due to Integration

During integration, shot noise due to the dark current i_{dc} and photocurrent i_{ph} dominates, with psd $S_{I_s}(f) = q(i_{ph} + i_{dc})$ A^2/Hz. To analyze noise generated during integration we again consider equation 3.5 but with the reset transistor turned off. If we assume that the photodiode capacitance is constant over the integration time, it is easy to show that the mean square value of the noise voltage sampled at the end of integration, *i.e.*, at t_{int}, is given by

$$\overline{V_n^2(t_{int})} = \frac{q(i_{ph} + i_{dc})}{C_{pd}^2} t_{int}. \tag{3.22}$$

The photodiode capacitance, however, is a function of its reverse bias voltage and can thus change significantly over integration time. So again we need to perform time-domain noise analysis.

Assuming that the noise is much smaller than the signal, we can write the noise part of equation 3.5 as

$$I_n(t) = I_s(t) = C_{pd}(v_{pd}(t))\frac{dV_n(t)}{dt} + g_c(t)V_n(t), \tag{3.23}$$

where

$$g_c(t) = -\frac{1}{C_{pd}(v_{pd}(t))}\frac{dC_{pd}(v_{pd}(t))}{dv_{pd}(t)}(i_{ph} + i_{dc})$$

is the varying capacitance induced conductance. Unlike the reset noise case, here we cannot ignore this conductance, because now v_{pd} varies in 1V range and thus $g_c(t)$ can be fairly large.

Equation 3.23 again is a general first order linear differential equation and the mean square value of V_n at the end of integration is given by

$$\overline{V_n^2(t_{int})} = q(i_{ph} + i_{dc}) \int_0^{t_{int}} \frac{1}{C_{pd}^2(v_{pd}(\tau))} e^{-2(i_{ph}+i_{dc})\int_\tau^{t_{int}} \frac{d(1/C_{pd}(v_{pd}(\tau_0)))}{dv_{pd}(\tau_0)} d\tau_0} d\tau. \tag{3.24}$$

Note that equation 3.22 follows from this more general equation if we assume that C_{pd} is constant during integration. To take the dependency of the photodiode

capacitance on the reverse bias voltage into consideration, we make the simplifying assumption of an abrupt pn junction to get that

$$C_{pd}(v_{pd}(t)) = C_{pd}(v_{pd}(0))\sqrt{\frac{v_{pd}(0)+\phi}{v_{pd}(t)+\phi}}, \tag{3.25}$$

where ϕ is the built in junction potential, and $v_{pd}(0)$ is the voltage on C_{pd} at the beginning of integration.

The signal part of equation 3.5 during integration can be written as

$$\frac{dv_{pd}(t)}{dt} = -\frac{i_{ph}+i_{dc}}{C_{pd}(v_{pd}(t))}. \tag{3.26}$$

Solving equation 3.26 we get that

$$v_{pd}(t) = v_{pd}(0) - \frac{(i_{ph}+i_{dc})}{C_{pd}(v_{pd}(0))}t + \frac{(i_{ph}+i_{dc})^2 t^2}{4C_{pd}^2(v_{pd}(0))(v_{pd}(0)+\phi)}. \tag{3.27}$$

The square term in equation 3.27 shows that the signal is actually reduced by the nonlinearity.

We can now explicitly express $C_{pd}(v_{pd}(t))$ as a function of t to get

$$C_{pd}(v_{pd}(t)) = C_{pd}(v_{pd}(0))\frac{1}{1-\frac{(i_{ph}+i_{dc})t}{2C_{pd}(v_{pd}(0))(v_{pd}(0)+\phi)}}. \tag{3.28}$$

Thus we have

$$\frac{d(1/C_{pd}(v_{pd}(t)))}{dv_{pd}(t)} = \frac{1}{C_{pd}(v_{pd}(0))}\frac{1}{2(v_{pd}(0)+\phi)-\frac{i_{ph}+i_{dc}}{C_{pd}(v_{pd}(0))}t}. \tag{3.29}$$

Substituting equations 3.27, 3.28, and 3.29 into equation 3.24, we get that the mean square noise voltage at the end of integration is given by

$$\overline{V_n^2(t_{int})} = \frac{q(i_{ph}+i_{dc})}{C_{pd}^2(v_{pd}(0))}t_{int}(1-\frac{1}{2(v_{pd}(0)+\phi)}\frac{i_{ph}+i_{dc}}{C_{pd}(v_{pd}(0))}t_{int})^2. \tag{3.30}$$

To demonstrate the effect of varying capacitance during integration, we consider

an example with $v_{pd}(0)$=2.1V, $C_{pd}(v_{pd}(0)) = 22fF$, i_{dc}=2.28fA, $\phi = 0.7$V, and $t_{int} =$ 30ms. These numbers are consistent with the parameters of our test structure circuit and experiments. Figure 3.6 and Figure 3.7 plot the signal $v_{pd}(t_{int})$ and the input referred RMS value of the noise as a function of the photocurrent i_{ph} for both constant and varying C_{pd}. Note that the effect of the nonlinearity is only pronounced for large signal values, and results in reduction of both the signal and the noise. The signal to noise ratio, however, improves as we shall see later. As technology scales or when employing certain high dynamic range schemes [5], the nonlinearity effects on SNR cannot be ignored.

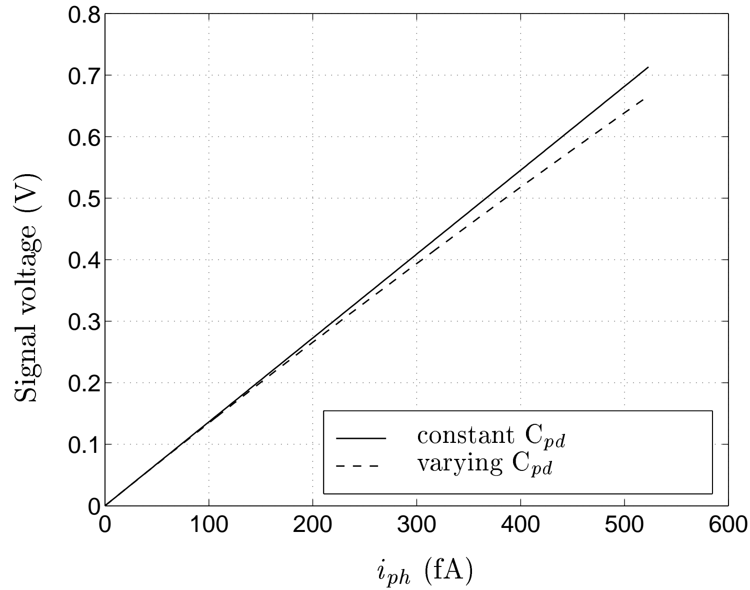

Figure 3.6: Signal voltage vs. photodiode current.

3.5 Noise Due to Readout

During readout, noise is due to transistors M2, M3, M4, and the column and chip level circuits thermal noise. Ignoring the noise contributions of the column and chip level circuits, which are very small, readout noise can be easily computed via the

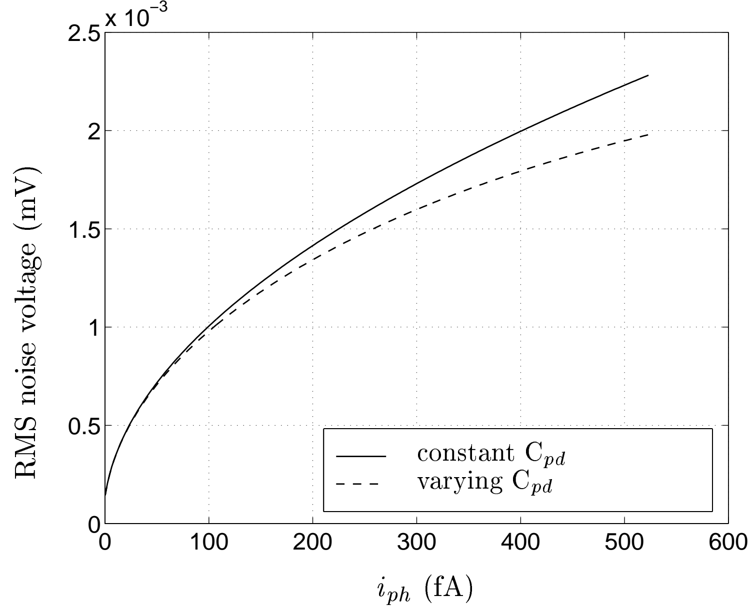

Figure 3.7: RMS noise voltage vs. photodiode current.

small signal circuit in Figure 3.8. In this figure, $I_{M2}(t)$, $V_{M3}(t)$, and $I_{M4}(t)$ are the thermal noise sources associated with M2, M3, and M4, respectively, g_{m2} and g_{m4} are the transconductances of M2 and M4, g_{d3} is the channel conductance of M3, and C_o is the column storage capacitance including the bitline capacitance. Assuming steady state, which is well justified here, it can be easily shown that the bitline referred mean square noise voltages due to M2, M3, and M4 are given by

$$\overline{V^2_{n,M2}} = \frac{2}{3}\frac{kT}{C_o}\frac{1}{1+\frac{g_{m2}}{g_{d3}}}, \tag{3.31}$$

$$\overline{V^2_{n,M3}} = \frac{kT}{C_o}\frac{1}{g_{d3}(\frac{1}{g_{d3}}+\frac{1}{g_{m2}})}, \text{ and} \tag{3.32}$$

$$\overline{V^2_{n,M4}} = \frac{2}{3}\frac{kT}{C_o}g_{m4}(\frac{1}{g_{d3}}+\frac{1}{g_{m2}}), \tag{3.33}$$

respectively. These equations show that different noise sources are associated with different noise bandwidth, and thus have different effects on the bitline referred noise.

To obtain more accurate results for noise during readout, we use SPICE. We

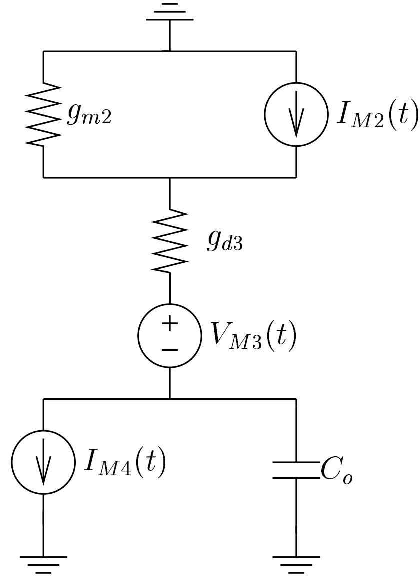

Figure 3.8: CMOS APS circuit noise model during readout.

sweep the IN voltage, perform DC analysis to determine the circuit bias point for each IN voltage value, and then perform ac noise analysis. Using this methodology, we simulated our APS circuit including the column and chip level circuits [59]. As expected, the noise contributions from column and chip level circuits were found to be very small. To compare the contributions of M2, M3, and M4 during readout we plot the simulated output referred psd for each in Figure 3.9. Note that except when the IN voltage is near its reset value, the noise from M3 is several orders of magnitude lower than the noise from M2 and M4. Summing up the contributions from the three transistors to the total output noise, we find that the output referred RMS noise voltage from the readout stage to be around 63μV, independent of the IN voltage value. Using the simulated IN to OUT voltage gain value of 0.81, this is equivalent to an input referred value of 78μV.

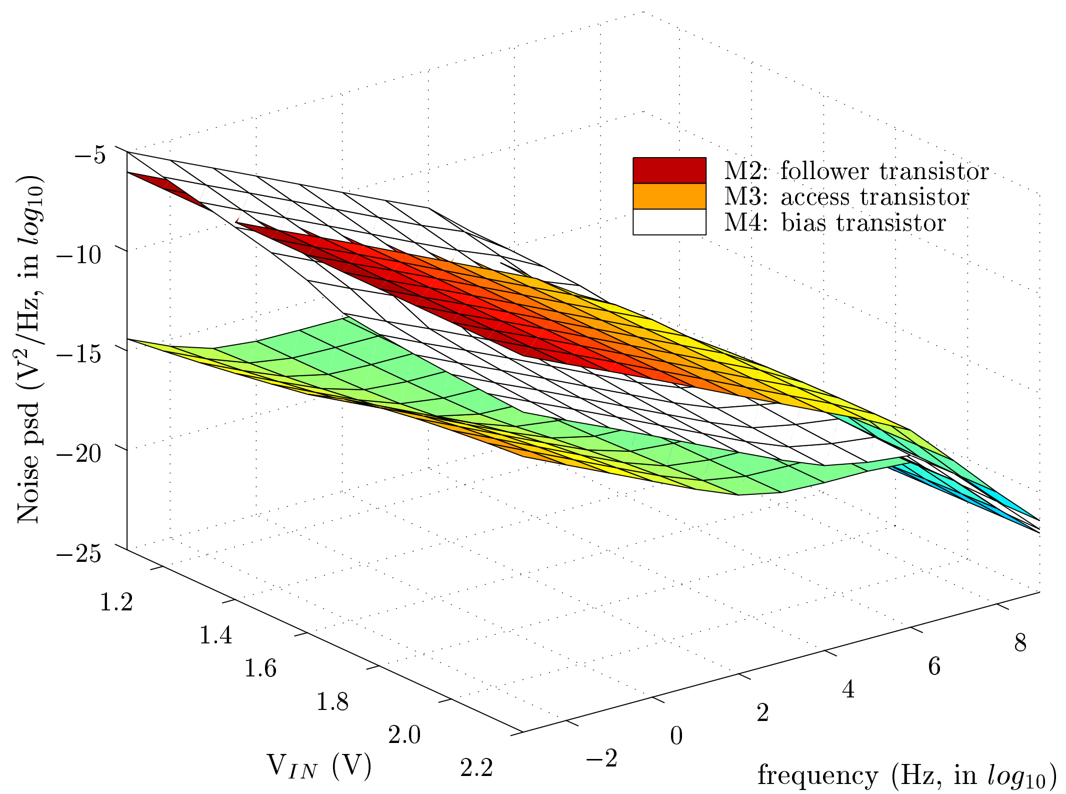

Figure 3.9: Readout noise power spectral density due to M2, M3, and M4.

3.6 Summary

We presented a detailed and rigorous analysis of thermal and shot noise in CMOS photodiode APS. We found that typical reset times are not long enough to achieve steady state. Using time-domain analysis, we found that reset noise is very close to $\frac{kT}{2C}$. This result, we believe, explains the discrepancy between measured reset noise and the commonly quoted $\frac{kT}{C}$ value. We proposed a new pseudo-flash reset method that alleviates image lag due to incomplete reset without increasing reset noise. We analyzed noise due to the photodetector shot noise taking nonlinearity into consideration and found that nonlinearity improves SNR at high illumination. For completeness, we also analyzed noise during readout using both hand analysis and SPICE simulation.

Chapter 4

Experiments

4.1 Introduction

Temporal noise is one of the most important parameters to measure when characterizing CMOS image sensors. To measure temporal noise a number of other sensor parameters must be determined first, including the sense node capacitance, readout circuit conversion gain and linearity, *etc.* Once these parameters are known, some other important image sensor characteristics, such as quantum efficiency, spectral response, and sensor array fixed pattern noise, can be readily estimated.

Techniques for characterizing CCD image sensors have been well established, which is excellently described by Janesick in [25]. In that paper the CCD transfer concept is introduced and used to characterize such parameters as charge transfer efficiency, quantum efficiency, linearity, gain, offset, signal to noise ratio, nonuniformity, dynamic range, and MTF. However, since the signal path for CMOS image sensors is quite different from CCDs, the CCD characterization models and techniques cannot be directly used for characterizing a CMOS image sensor. For example, in a typical CCD sensor all pixels share the same output amplifier, and thus the output voltage can be expressed as a linear function of the photogenerated charge plus shot noise and readout noise, assuming constant gain across the pixels. As a result, differences between pixel responses are primarily due to differences in their photodetector characteristics, which are usually very small. By comparison, the output response for a

CMOS APS can exhibit significant nonlinearity[14], and pixel to pixel gain and offset variations, due to the presence of the column and pixel amplifiers which are not shared by all pixels[32].

In this chapter, we describe the method to characterize CMOS APS. Similar to Janesick's photon transfer method, we rely on the Poisson statistics of shot noise to estimate the sense node capacitance, and thus the conversion gain. The difference is that here we take into consideration the CMOS APS output response nonlinearity, pixel to pixel gain and offset variations, and readout noise. Using this method we measure the capacitance, conversion gain, linearity, offset, quantum efficiency, spectral response, fixed pattern noise, and temporal noise, for the test structures fabricated in 0.35μ standard CMOS processes. We find that the measured reset noise mean square value is indeed close to $\frac{kT}{2C}$, as derived in chapter 3. The measured SNR value also matches well with our analysis. We also demonstrate the incomplete reset induced image lag.

The remainder of the chapter is organized as follows. In Section 4.2 we describe the experiment setup, and the procedure we used to characterize CMOS image sensors. In section 4.3, we present our experimental results of temporal noise in the CMOS APS test structures.

4.2 Experiment Setup and Procedure

The experiment setup for characterizing CMOS APS sensors is shown in Figure 4.1. The optical part of the setup consists of a DC regulated tungsten halogen light source, a monochromator, an integrating sphere, and a calibrated photodiode. The monochromator is controlled by a PC. The output of the integrating sphere is used to provide the needed uniform illumination to the image sensor. The electrical part of the setup consists of a pattern generator, a logical analyzer, highly regulated power supply, and a device under test (DUT) board. The DUT board holds the test structure sensor chip, a low noise amplifier, an analog to digital converter, some analog bias circuits, and digital control signal interface. All of the electrical equipments and the monochromator are GPIB programmable.

A similar setup has been used to characterize digital pixel CMOS image sensors. To test DPS, the optical part of the setup described in previous paragraph can be kept the same, while the electrical part needs some modification. In this case, the pattern generator is replaced by a field programmable gate array (FPGA) board, and the logical analyzer is replaced by an image capture board.

To accurately measure the sensor parameters, special care has been taken to minimize the environmental interference such as light source fluctuations, temperature fluctuations, electromagnetic interference, *etc.* We housed the setup in a well air conditioned dark room. We used a light source with intensity fluctuations of less than 0.5%. The ripple of the dc power supply was limited to be less than 0.2%. Temperature and light intensity were recorded each time data was taken. We remotely performed all the experiments to minimize the human interference.

The analog sensor output is amplified using the on board low noise amplifier and then quantized using an on board 16-bit ADC. The digital number is then collected by a logical analyzer, and finally transfered to a computer. All the critical analog signals are coaxed to shield the environmental interference.

To measure the sense node capacitance, and hence the conversion gain, the sensor is irradiated by a monochromatic light source through the integrating sphere. In the measurements, instead of varying illumination (common in CCD methods), illumination is kept constant and the pixel output is continuously observed and sampled at regular time intervals during integration time. Using this method the effect of amplifier offsets can be eliminated, and the nonlinearity of the sensor response can be approximated by a piecewise linear response. The experiment is repeated multiple times to obtain good estimates of the pixel output mean and variance at each sample time. The sensor response is approximated by a piecewise linear function. Using the Poisson statistics of shot noise, which is also used in the CCD method, the system conversion gain, collected charge, and read noise are estimated for each line segment. This procedure is repeated at no illumination so that dark current generated charge may be estimated and subtracted from the total charge estimates.

Now we describe the method quantitatively. Let N be the number of the independent experiments we performed. Each experiment started with reseting the sensor,

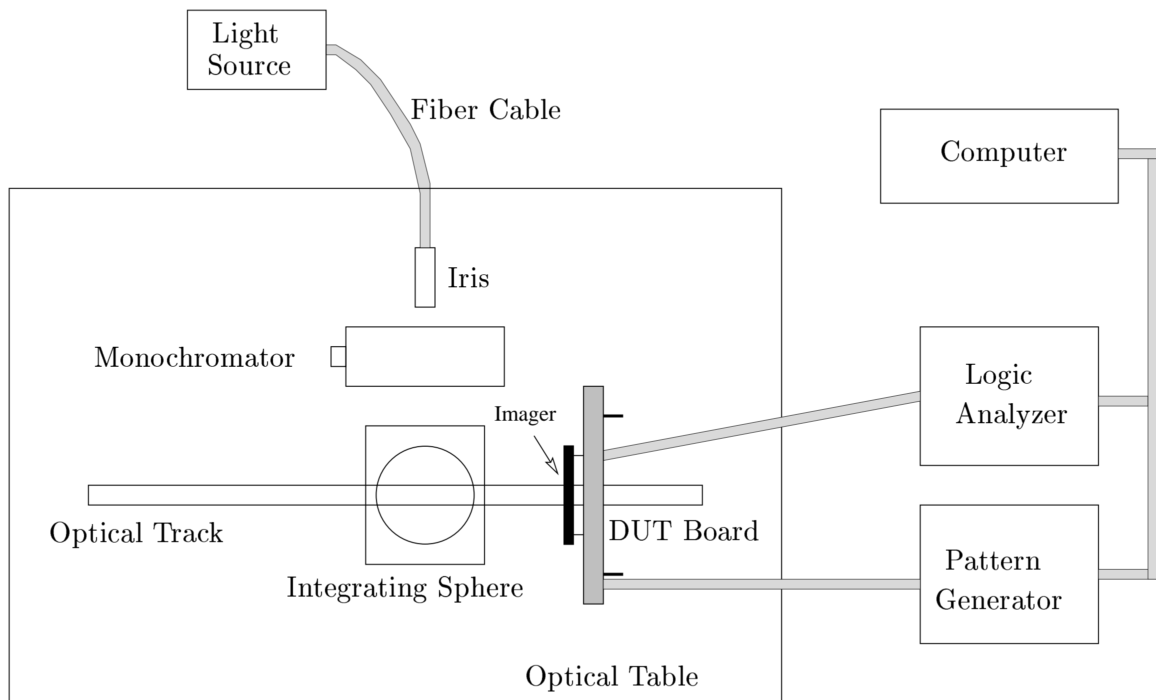

Figure 4.1: Experiment setup for CMOS image sensors characterization.

and then contiously sampled the pixel output. Let M be the samples we took in each experiment. We denote the samples by $V_{i,j}$, $i = 1, \ldots, N$ and $j = 1, \ldots, M$. We approximate the nonlinear sensor response using a piecewise linear model consisting of $K \geq 1$ segments. For each set of voltage output samples $V_{i,j}$, $j = 1, \ldots, M$, the first segment ranges from $j = j_0 = 1$ to j_1, the second from $j = j_1$ to j_2, and the last from j_{K-1} to $j_K = M$. The number of segments K is determined as follows. We first investigate several output sample paths, and then choose a K which is large enough to provide a good fit, but small enough that the number of samples per segment is sufficient for data analysis. The pixel output within segment s, $0 \leq s \leq K-1$ is given by:

$$V_{i,j} = g_s Q_{i,j} + U_{s,i} + Z_{i,j}, \tag{4.1}$$

where g_s is the conversion gain from the pixel to the sensor output for segment s measured in volts/electron, $Q_{i,j}$ is the total charge (in electrons) collected at the jth sample time (of path i), $U_{s,i}$ is the offset of path i in segment s and is assumed to be random with unknown mean and variance. The charge $Q_{i,j}$ is the sum of the photo-generated charge $Q^l_{i,j}$ and leakage or dark charge $Q^d_{i,j}$. $Z_{i,j}$ is the readout noise which is assumed to be independent and identically distributed for all i and j, with zero mean and unknown variance σ^2_Z. The readout noise is also assumed to be independent of the charge samples $Q_{i,j}$, and the offsets $U_{s,i}$. Note that the gain g_s can vary from pixel to pixel. The following discussion will consider the output from a fixed pixel. After the measurements and analysis are repeated for all pixels in the image sensors, we can further estimate the gain and offset fixed pattern noise.

To eliminate the offset we normalize with respect to the first sample in each segment to get that

$$X_{s,i,(j-j_s)} = g_s(Q_{i,j} - Q_{i,j_s}) + Z_{i,j} - Z_{i,j_s}, \tag{4.2}$$

where $j = j_s + 1, \ldots, j_{s+1}$.

The charge increments $Q_{i,j} - Q_{i,j_s}$ are samples from a Poisson process and thus

are Poisson random variables with mean and variance equal to

$$\mu^l(j-j_s)\tau + \mu^d(j-j_s)\tau,$$

where μ^l is the average photocurrent, μ^d is the average dark current, and τ is time interval between two consecutive samples. Thus, the mean and variance of the sample $X_{s,i,(j-j_s)}$ are given by:

$$E[X_{s,i,(j-j_s)}] = g_s(\mu^l + \mu^d)(j-j_s)\tau, \tag{4.3}$$

and

$$Var[X_{s,i,(j-j_s)}] = g_s^2(\mu^l + \mu^d)(j-j_s)\tau + 2\sigma_Z^2, \tag{4.4}$$

respectively.

Note that the sample means and variances can be estimated using

$$\overline{X_{s,j}} = \frac{1}{N}\sum_{i=1}^{N} X_{s,i,j}, \text{ and} \tag{4.5}$$

$$\overline{\sigma_{s,j}^2} = \frac{1}{N-1}\sum_{i=1}^{N}\left(X_{s,i,j}^2 - \overline{X_{s,j}}^2\right), \tag{4.6}$$

where $j = 1, \ldots, j_{s+1} - j_s$.

The charge collected in segment s is then estimated as

$$\overline{Q_s^l} = \frac{\left(g_s\overline{(\mu^l+\mu^d)\tau}\right)^2}{\left(g_s^2\overline{(\mu^l+\mu^d)\tau}\right)}(j_{s+1}-j_s). \tag{4.7}$$

The same set of measurements and analysis is repeated under dark condition to obtain an estimate of the dark charge in segment s

$$\overline{Q_s^d} = \frac{\left(g_s\overline{(\mu^d)\tau}\right)^2}{\left(g_s^2\overline{(\mu^d)\tau}\right)}(j_{s+1}-j_s). \tag{4.8}$$

Now let $\overline{X_{s,(j_{s+1}-j_s)}^p}$ be the mean output value of pixel p in segment s at the last

sample $(j_{s+1} - j_s)$, then

$$\overline{g_s^p} = \frac{T\overline{X^p_{s,(j_{s+1}-j_s)}}}{(j_{s+1} - j_s)\tau \sum_{s=0}^{K-1}(\overline{Q_s^l} - \overline{Q_s^d})}, \tag{4.9}$$

where T is the total integration time.

Once conversion gain is determined, we can measure the sensor fixed pattern noise (FPN) and quantum efficiency (QE). FPN measurements involve irradiating the sensor with uniform light and analyzing the intensity variations of the supposedly uniform output images. Uniform irradiation is achieved by first shining the light source into an integrating sphere. The uniform light emitted from the exit port of the integrating sphere is then used to irradiate the sensor.

QE is the fraction of photon flux that contributes to the photocurrent in a photodetector or in a pixel. To measure QE, the photon flux incident on the sensor must be determined. The experiment setup is almost identical to that of FPN measurements. The only additional step here is that, after collecting measurements with the chip, the sensor chip is moved aside and a calibrated photodiode is placed at the same position as the sensor chip, to measure incident light intensity. The spectral response curve of the image sensor can be obtained by the procedure used to estimate QE. We only need to illuminate the sensor with a monochromatic light source placed in front of the integrating sphere and estimate QE at each wavelength of light. Note that in FPN, QE, and spectral response measurements, the experiments must be repeated many times under the same condition, to remove the temporal noise.

To measure the temporal noise, we only pick a group of representative pixels that have normal QE and spectral response. The output value of these pixels must be close to the average output value of all pixels when the sensor is irradiated with uniform light. By doing so, we can reduce the amount of data to be processed, and can increase the measurement accuracy. The experiment is again repeated many times under the same condition, and the temporal noise is calculated using the variance estimator. The requirement of removing environmental interference is most strict in noise measurements, because the interference can often overwhelm the “true” noise one intended to measure.

4.3 Experimental Results

Using the setup described in the previous section, we characterized APS and DP-S fabricated in several different CMOS processes by several different semiconductor foundries. In this section, we present the characterization results obtained from a 64×64 APS test structures[59], which were fabricated in a 0.35μ standard digital CMOS process. A summary of the main sensor characteristics are provided in Table 4.1.

Technology	0.35 μm, 4-layer metal 1-layer poly, nwell CMOS
Number of Pixels	64×64
Pixel Area	14μm×14μm
Transistors per pixel	3
Fill Factor	29%
Photodetector	nwell/psub diode
Pixel Interconnect	Metal1 and Poly

Table 4.1: 64×64 CMOS APS Test Structure Characteristics.

The output of a typical pixel irradiated with 1.76×10^{12} photons/(s·cm^2) at $\lambda =$ 600nm is shown in Figure 4.2. As the output of CMOS APS is nonlinear in the integration time, we used 3 linear segments to approximate the reponse. The first segment consisted of 80 samples, while the second and third consisted of 81 samples each. The APS output mean and variance as a function of time, after this linearization are shown in Figures 4.3 and 4.4 respectively.

From these experiments, the sense node capacitance was estimated to be 22fF at reverse bias of 2V. Conversion gain, QE, spectral response, and FPN were then measured, as reported in [12] and [7]. We used the results to pick the representative pixels for noise measurement

In taking the noise measurements we first determined the board level noise, including the LNA noise and ADC quantization noise. This was done by directly driving the node OUT with a low noise DC voltage source. The measured output referred RMS noise voltage was found to be 82 μV, which is comparable to the simulated readout stage noise, but much lower than the reset noise. As a result reset noise can

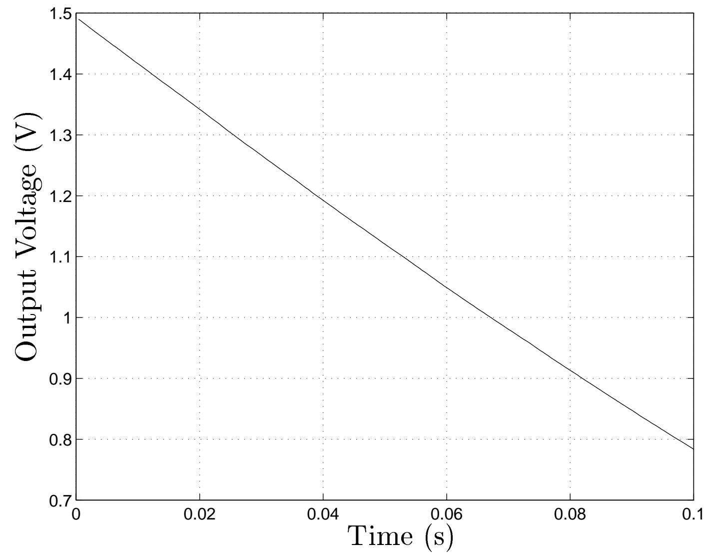

Figure 4.2: CMOS APS output waveform

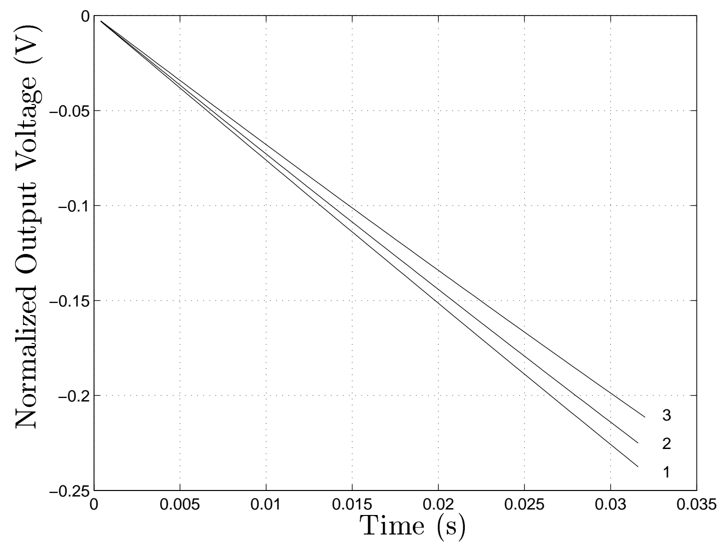

Figure 4.3: CMOS APS output mean as a function of time for segments 1, 2, and 3.

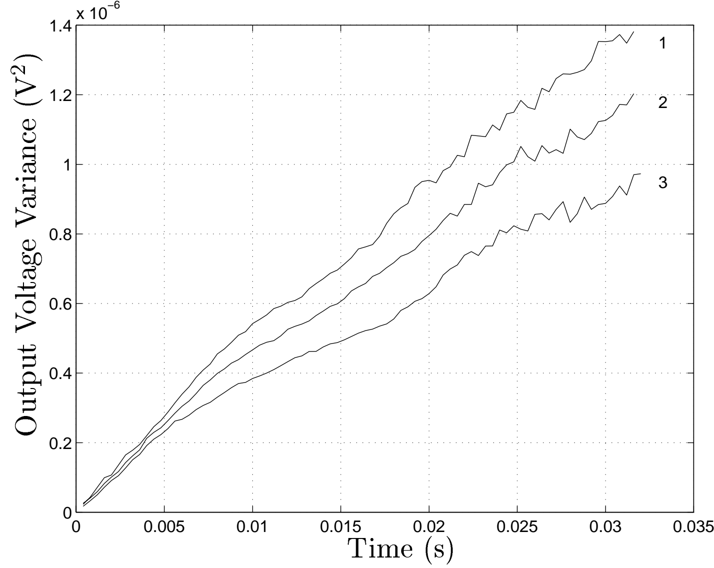

Figure 4.4: CMOS APS output variance as a function of time for segments 1, 2, and 3.

still be accurately measured.

To measure the reset noise we reset the pixel and sample the output voltage twice. The two samples are designated as S_1 and S_2 respectively. Each sample contains two noise components, the reset noise and the other noise. The two noise components are generated by different devices and thus are independent of each other. Hence for every sample we get that

$$\sigma_S^2 = \sigma_{reset}^2 + \sigma_{other}^2.$$

Note that for each sample pair, the reset noise is fully correlated, while the other noise is totally uncorrelated. We then subtract one sample from the other within the pair, *i.e.*, $S' = S_1 - S_2$, and repeat the measurement and procedure many times. The variance of S' is simply the noise power of the other noise components, *i.e.*,

$$\sigma_{S'}^2 = \sigma_{other}^2.$$

Thus the reset noise power is found to be

$$\sigma_{reset}^2 = \sigma_S^2 - \sigma_{S'}^2.$$

Using this method, the RMS reset noise voltage was estimated to be 262μV, while RMS of the other noise voltage was estimated to be 113μV. Applying the IN to OUT voltage gain of 0.81, we get an estimated input referred RMS reset noise voltage of 323μV, which is very close to the 303μV given by $\sqrt{\frac{kT}{2C_{pd}}}$, and much lower than the $\sqrt{\frac{kT}{C_{pd}}}$ value of 428μV. The experiment was repeated at several reset times ranging from 1 μs to 10 μs and under several low illumination levels, and the same results were obtained.

We also measured the overall RMS noise voltage at different signal levels. In Figure 4.5 we plot the measured and the calculated signal to noise ratios (SNR) versus the output signal. Two calculated SNR curves are given, one assuming constant photodiode capacitance and the other assuming varying photodiode capacitance as discussed in section 3.4. Note that the measured SNR curve is very close to the calculated curve assuming varying capacitance, but that the curve assuming constant capacitance becomes slightly lower than the others at high illumination levels.

To illustrate the image lag caused by incomplete reset as described in section 3.3, we performed experiments under dark and bright conditions. In Figure 4.6 we plot the measured final reset voltage averaged over many trials and the simulated photodiode voltage (as indicated by the dashed lines) for five consecutive frames. The figure confirms that lag occurs following a dark frame. We repeated the bright experiment under several illumination levels and did not observe any image lag.

4.4 Summary

We described the setup and the methods we used to characterize the CMOS APS. In addition to using the shot noise statistics of photons, We take into consideration the nonlinear sensor response and large FPN. We then characterized the 64×64 CMOS APS test structure fabricated in a 0.35μ standard digital CMOS process. We found

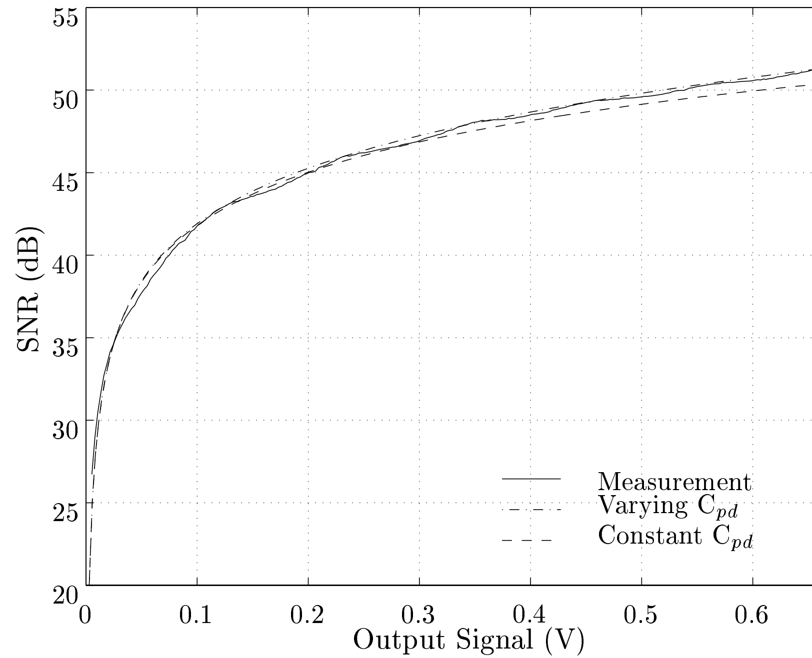

Figure 4.5: Simulated vs. measured signal to noise ratio.

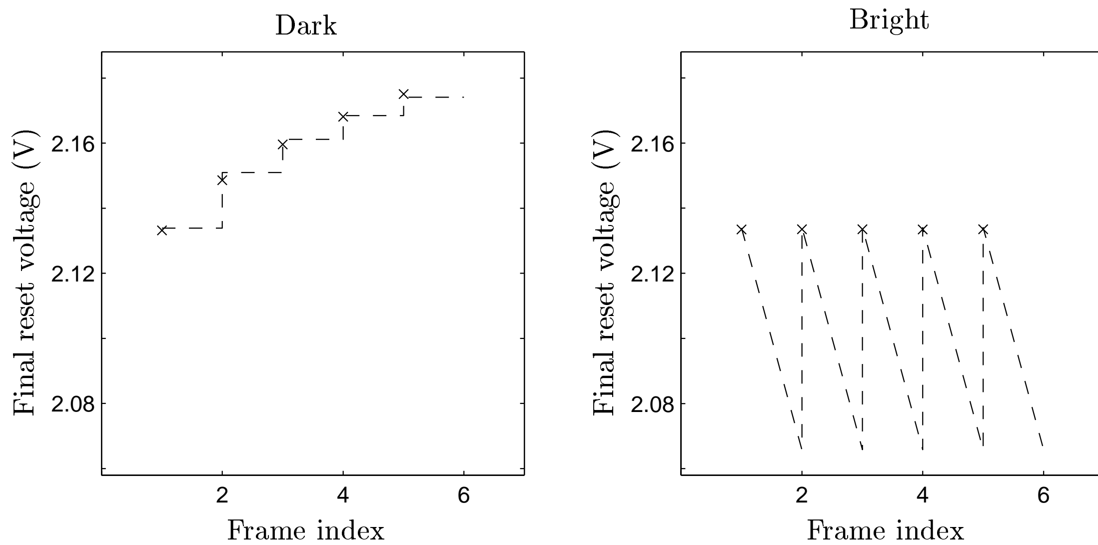

Figure 4.6: Measured final reset voltage for five consecutive frames (indicated by $\times$), and the simulated photodiode voltage waveform (indicated by the dashed lines).

that the measured reset noise is indeed very close to the half kT/C result derived in previous chapter. The measured SNR is also consistent to the calculated shot noise using the nonlinear model we developed in previous chapter.

Chapter 5

MOSFET 1/f Noise Models

5.1 Introduction

The analysis of 1/f noise in CMOS APS is typically performed in frequency domain, using the standard 1/f noise model. A low cutoff frequency is typically used to get reasonable noise power estimates. The choice of this low cutoff frequency is quite arbitrary, however, and can cause significant inaccuracy in estimating noise power. So in this chapter, we start from the first principles to derive a 1/f noise model that is more suitable for analyzing 1/f noise in CMOS APS.

Historically, 1/f noise in MOSFETs has been of concern mainly in the design of low frequency linear analog circuits such as bias circuits, audio amplifiers, *etc.* [16]. As CMOS technology scaled down to the submicron regime, 1/f noise has become of greater concern in a wider range of circuit designs. Scaling has enabled the use of CMOS technology in many new applications such as RF circuits and CMOS image sensors that are quite sensitive to 1/f noise. Moreover, as mentioned in [20] 1/f noise in MOSFETs increases rapidly with technology scaling. As a result it is becoming more important to be able to accurately estimate the effect of 1/f noise for a wide variety of circuits.

Analysis of 1/f noise in MOSFET circuits is typically performed using the well established stationary 1/f noise model [22, 24], which henceforth will be referred to as the standard 1/f noise model. Recent experimental results, however, show that the

estimates using this standard model can be quite inaccurate especially for switched circuits. An important class of such circuits is the periodically switched circuits, which are widely used in RF applications, such as switched capacitor networks, modulators and demodulators, and frequency converters. In the simplest case of such circuits, which involves only a periodically switched transistor, it was shown that the measured drain voltage 1/f noise psd [1, 6, 15] is much lower than the estimates using the standard 1/f noise model. Another example that has recently been receiving much attention is 1/f-induced phase noise in CMOS oscillators [18, 17, 40]. Unlike the amplitude fluctuations, which can be practically eliminated by applying limiters to the output signal, phase noise cannot be reduced in the same manner. As a result, it limits the available channel in wireless communication. Recent measurements [15] show that the 1/f-induced phase noise power spectral density (psd) in ring oscillators is much lower than the estimate using the standard 1/f noise model.

In this chapter, we propose a nonstationary extension of the standard 1/f noise model, which accurately models 1/f noise when the transistor is switched from the off to the on state. The model is based on the fact that when the MOSFET is off the active traps are mostly empty. By modifying the random telegraph signal (RTS) model for a single trap to reflect this fact, the noise autocovariance function is derived. We will then show that this nonstationary model can be used to obtain accurate estimates of the effect of 1/f noise in switched circuits. In particular we consider the aforementioned example circuits.

The rest of the chapter is organized as follows. In section 5.2 we review the standard 1/f noise model. In section 5.3 we present our nonstationary extension. In sections 5.4 and 5.5 we use our nonstationary model to estimate the effect of 1/f noise on a periodically switched transistor, and ring oscillator, respectively. In both cases we find that our estimates are consistent with the reported measurement results.

5.2 Standard 1/f Noise Model

1/f noise (sometimes also called flicker noise, or low frequency noise), in the strictest sense, refers to the noise whose power spectral density (psd) is inversely proportional

to frequency, *i.e.*, $S_N \propto \frac{1}{|f|}$. More generally, noise with $S_N \propto \frac{1}{|f|^\beta}$, for $\beta > 0$, is also called 1/f noise (or 1/f like noise). In addition to electronic devices, 1/f noise also appears in many other devices and natural phenomena, such as oscillation of quartz crystals, geophysical records, economic data, traffic-flow rates, image texture, heart beat rates, ..., just to name a few. As a result, the origin of 1/f noise has been the subject of numerous studies in many different fields. Unfortunately, since 1/f psd is not integrable, it is not a valid psd of stationary processes and there is no agreed upon universal mathematical or physical model to describe it.

In this thesis we are mainly concerned with 1/f noise in MOS transistors. Over the last three decades, two main theories of 1/f noise in MOS transistors were developed, namely the carrier number fluctuation theory, and the mobility fluctuation theory [54]. The carrier number fluctuation theory attributes 1/f noise to random capture and emission of conduction channel carriers by traps in the gate oxide, while the mobility fluctuation theory considers the 1/f noise as a result of the fluctuation in the carrier mobility. Both theories succeeded in partially explaining some of the experimental data. However, since it was very difficult to experimentally verify the noise generation mechanism, there was no conclusive evidence to support either theory.

This controversy has, to a large extent, been resolved by recent studies of small area sub-micron MOS transistors. In these transistors, very few, (sometimes only one) traps are active in the gate oxide. Capture and emission of channel carriers by this trap are represented by the trapped electron number $N(t)$, which takes the value 1 if a carrier is captured and zero otherwise, as depicted in Figure 5.1. The trap is active when its energy level is close to the Fermi level [28] in the bulk. In this case the capture and emission rates must be nearly equal. Thus, $N(t)$ can be modeled as a Random Telegraph Signal (RTS) with rate λ. In equilibrium, the autocovariance of $N(t)$ is given by

$$\mathcal{C}_\lambda(\tau) = \frac{1}{4}e^{-2\lambda\tau},$$

and the corresponding double sided power spectral density (psd) is

$$S_\lambda(f) = \frac{1}{4}\frac{\lambda}{\lambda^2 + (\pi f)^2}.$$

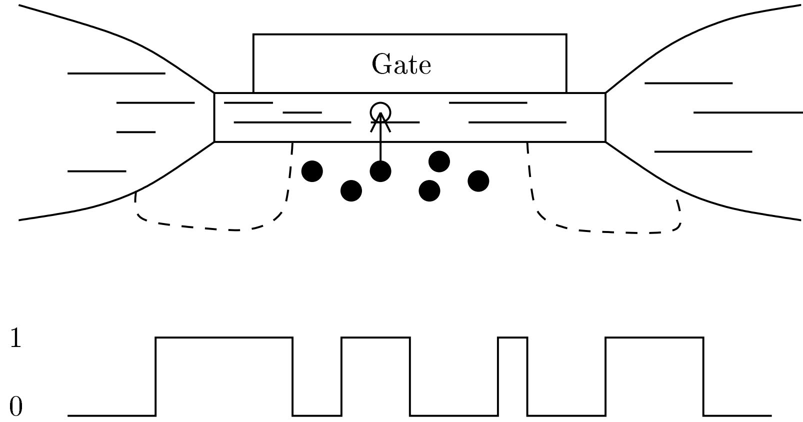

Figure 5.1: MOSFET with single trap in its gate oxide (top) and the resulting trapped electron number $N(t)$ waveform (bottom).

In practical MOSFETs there can be many traps in the gate oxide. Since each trap captures and emits carriers independently, the psd of the total trapped electron number is the sum of the psds for the individual trapped electron numbers. Traps can have different rates depending on their location in the gate oxide. The distribution of the rates is believed to obey a log uniform law [53]

$$g(\lambda) = \frac{4kTAt_{ox}N_t}{\lambda \log \frac{\lambda_H}{\lambda_L}}, \tag{5.1}$$

where kT is the thermal energy, A is the channel area, t_{ox} is the effective gate oxide thickness, N_t is the trap density (in $\mathrm{eV}^{-1}\mathrm{cm}^{-3}$), λ_H is the fastest transition rate or high corner frequency , and λ_L is the slowest transition rate or low corner frequency. The corner frequencies are related to t_{ox} through the equation $\log \frac{\lambda_H}{\lambda_L} = \gamma t_{ox}$, where γ is the tunneling constant. The psd of the total trapped electron number is thus given by

$$\begin{aligned} S(f) &= \int_{\lambda_L}^{\lambda_H} S_\lambda(f) g(\lambda) d\lambda \\ &\approx \frac{kTAN_t}{2\gamma f}, \text{ for } \lambda_L < f < \lambda_H. \end{aligned} \tag{5.2}$$

For $f < \lambda_L$, $S(f)$ is constant and for $f > \lambda_H$ it is $\propto \frac{1}{f^2}$. In Figure 5.2 we plot the psd of the total trapped electron number, as well as the trapped electron number psds of three individual traps with highest, slowest, and intermediate transition rate respectively. As can be seen, at practical frequency range, the psd of the total trapped electron number is indeed inversely proportional to the frequency, as the name 1/f noise indicates. At extremely high frequency, however, the psd falls with square of the frequency, where only slow traps contribute noise. At very low frequency, the psd becomes a constant, as fast traps now dominate the total noise. Note that because the psd becomes flat at low frequency, the integration of psd over all frequency is not infinity, which solves the infinite noise power problem that has bothered the 1/f noise researchers for long time.

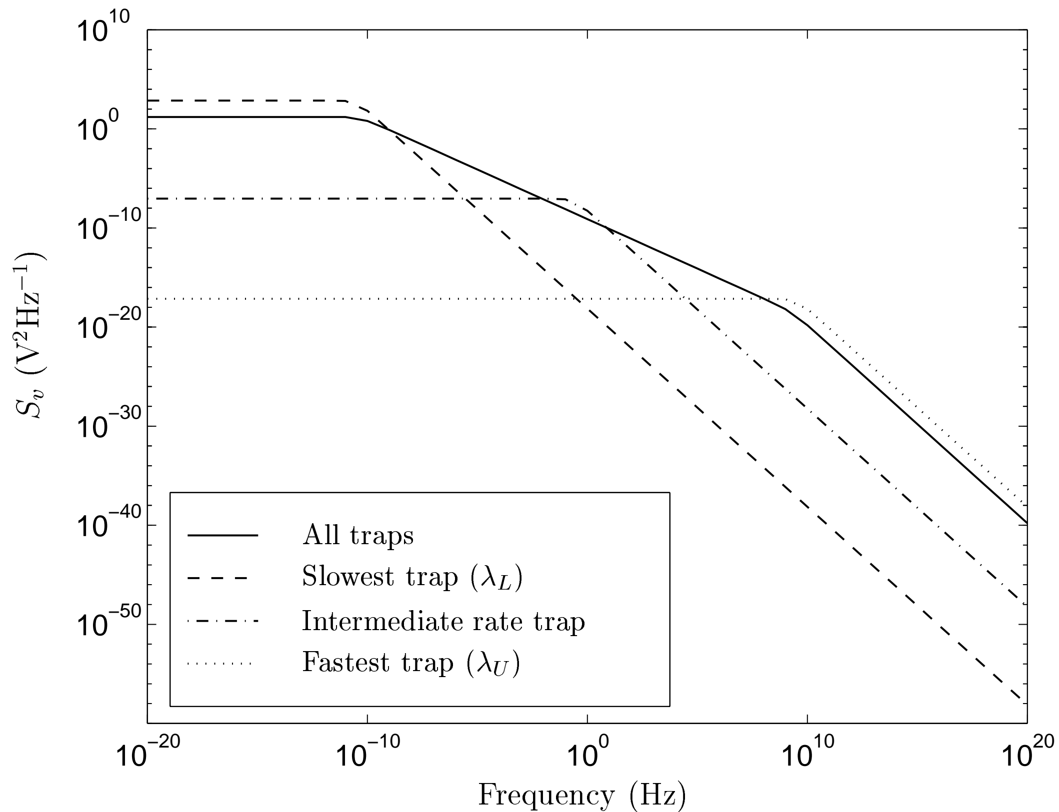

Figure 5.2: 1/f noise psd as the summation of psds due to multiple traps.

The MOSFET charge-control analysis can then be used together with the derived psd of the total trapped electron number to find the 1/f noise psd of the drain current. For submicron n-channel MOSFET, carrier number fluctuations dominate [4, 2] and the equivalent 1/f noise psd of the drain current is given by

$$S_{I_d}(f) = g_m^2 S_{V_g}(f) = g_m^2 \frac{1}{C_{ox}^2} S_{Q_{ch}}(f) = g_m^2 \frac{1}{C_{ox}^2} (\frac{q}{A})^2 S(f) = \frac{g_m^2 q^2 kTN_t}{2C_{ox}^2 A\gamma f}, \tag{5.3}$$

where C_{ox} is the gate oxide capacitance, g_m is the transconductance, $S_{V_g}(f)$ is the equivalent gate voltage 1/f noise psd, and $S_{Q_{ch}}(f)$ is the channel charge density 1/f noise psd. Note that $S_{I_d}(f)$ is inversely proportional to the gate area, which explains the reason why 1/f noise is becoming more pronounced as technology scales.

Circuit designers typically use the SPICE 1/f noise model

$$S_{V_g}(f) = \frac{k_F}{2C_{ox}Af},$$

and are given the value of the SPICE 1/f noise parameter k_F. From equation 5.3, we find that

$$k_F = \frac{q^2 kTN_t}{C_{ox}\gamma}.$$

A unified number and mobility theory [22] can be used to extend these results to p-channel MOSFETs.

5.3 Nonstationary 1/f Noise Model

In this section, we present our nonstationary extension of the standard 1/f noise model discussed in the previous section. The main purpose of the extension is to be able to more accurately analyze 1/f noise in switched circuits. We begin by considering the case of a single trap in an n-channel MOSFET. The key observation that led to our extension is that with very high probability the trap is empty when the transistor is off. The physical reason can be explained via the MOSFET energy band diagram in Figure 5.3. The energy levels E_t^o and E_t represent the trap energy in the off and on states, respectively. Note that for the trap to be active when the transistor is on E_t

must be very close to E_f, *i.e.*, $E_t \approx E_f$. When the transistor is turned on the trap energy shifts down by several hundred millivolts, which is the same as the shift in the surface potential. This is the case since the difference between the energy level of the trap and that of the oxide conduction band is independent of the gate bias voltage. This means that $E_t^o - E_t \gg kT$. It is well known [28] that the ratio of the trap capture rate λ_c to its emission rate λ_e is exponentially related to the difference between the trap energy and the Fermi level. When the transistor is off, this gives that

$$\frac{\lambda_c}{\lambda_e} = \exp(\frac{E_F - E_t^o}{kT}) \ll 1.$$

Thus with very high probability, the trap is empty when the transistor is off. If we let $t = 0$ denote the time when the transistor turns on, we get that $N(0) \approx 0$.

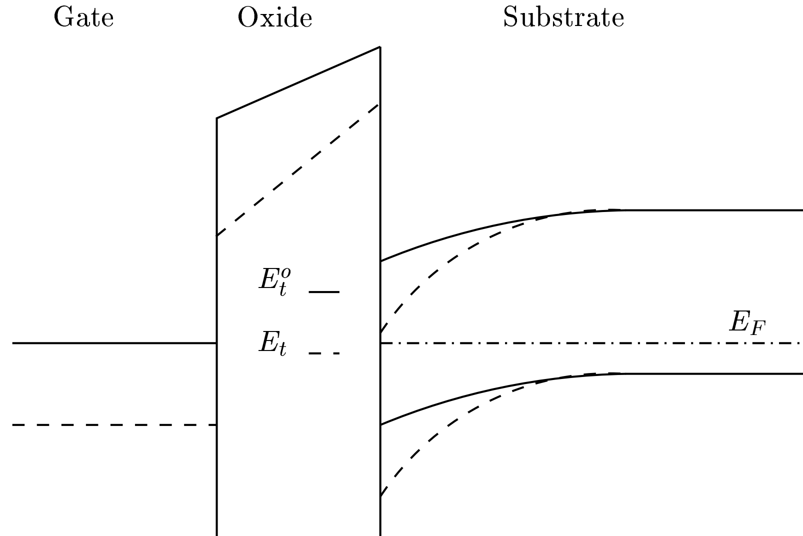

Figure 5.3: Energy-band diagram for MOSFET, with an active trap inside its gate oxide. Solid lines are used when the transistor is off, and dashed lines are used when the transistor is on.

Now let $p_1(t)$ be the probability that the trap is occupied at time $t > 0$, and let $p_{1,1}(t, \tau)$ be the probability that the trap is occupied at time $t + \tau$ ($\tau > 0$), given that

it is occupied at time t. The autocovariance function of $N(t)$ is then given by

$$\mathcal{C}_\lambda(t,\tau) = p_1(t)p_{1,1}(\tau) - p_1(t)p_1(t+\tau)$$

To find $p_1(t)$ we note that

$$p_1(t+\Delta t) = p_1(t)(1-\lambda\Delta t) + (1-p_1(t))\lambda\Delta t. \tag{5.4}$$

Thus in the limit

$$\frac{dp_1(t)}{dt} + 2\lambda p_1(t) = \lambda. \tag{5.5}$$

Solving for p_1 we get that

$$p_1(t) = \frac{1}{2}(1-e^{-2\lambda t}). \tag{5.6}$$

To find $p_{1,1}(t,\tau)$ we let $p_{1,0}(t,\tau)$ be the probability that the trap is empty at time $t+\tau$ ($\tau > 0$), given that it is occupied at time t. Note that $p_{1,0}(t,\tau) = 1 - p_{1,1}(t,\tau)$, and that

$$p_{1,1}(t+\tau+\Delta\tau) = p_{1,1}(t,\tau)(1-\lambda\Delta\tau) + p_{1,0}(t,\tau)\lambda\Delta\tau. \tag{5.7}$$

Thus in the limit

$$\frac{dp_{1,1}(t,\tau)}{d\tau} + 2\lambda p_{1,1}(t,\tau) = \lambda. \tag{5.8}$$

Solving for $p_{1,1}$ we get that

$$p_{1,1}(t,\tau) = p_{1,1}(\tau) = \frac{1}{2}(1+e^{-2\lambda\tau}). \tag{5.9}$$

Therefore the autocovariance function of $N(t)$ is given by

$$\begin{aligned}\mathcal{C}_\lambda(t,\tau) &= p_1(t)p_{1,1}(\tau) - p_1(t)p_1(t+\tau) \\ &= \frac{1}{4}e^{-2\lambda\tau}(1-e^{-4\lambda t}).\end{aligned} \tag{5.10}$$

As $t\to\infty$, $\mathcal{C}_\lambda(t,\tau) \to \frac{1}{4}e^{-2\lambda\tau}$, which is the stationary autocovariance function derived in the previous section.

The autocovariance of the total trapped electron number is simply the sum of the

autocovariances for the individual traps in the gate oxide, *i.e.*,

$$\mathcal{C}(t,\tau) = \int_{\lambda_L}^{\lambda_H} \mathcal{C}_\lambda(t,\tau) g(\lambda) d\lambda.$$

Applying charge-control analysis, we get the resulted mean square gate voltage as

$$\overline{V_g^2(t)} = (\frac{q}{AC_{ox}})^2 \int_{\lambda_L}^{\lambda_H} \mathcal{C}_\lambda(t,0) g(\lambda) d\lambda. \quad (5.11)$$

This integral does not have a closed form solution, and must be evaluated numerically.

We now compare the 1/f noise power computed using the conventional frequency domain method to the more accurate time domain method described. For the comparison and for the remainder of the thesis we assume a 0.35μm CMOS technology with $t_{ox} = 7$nm, $\gamma = 10^8$cm^{-1}, $\lambda_H = 10^{10}$s^{-1}, and $N_t = 10^{17}$eV^{-1}cm^{-3}. Using these parameter values we get $\lambda_L = 4 \times 10^{-21}$, $C_{ox} = 5$fFμm^{-2}, and $k_F = 5 \times 10^{-24}$V^{2}F at $T = 300$K.

In Figure 5.4, we plot the RMS gate voltage $\sqrt{\overline{V_g^2}}$ due to the 1/f noise as a function of the circuit on-time t_{on} using both the standard model and our nonstationary extension. Shown in the bottom half of the figure is the error using the standard model as a percentage, referred to the result using the nonstationary model. As expected the error percentage decreases as t_{on} increases. In this example, we assume that the channel area $A = 1\mu m^2$.

5.4 1/f Noise in a Periodically Switched Transistor

Periodically switched circuits are widely used in RF applications, such as switched capacitor networks, modulators and demodulators, and frequency converters. Unlike linear circuitry, these circuits typically undergo large signal periodic variations in their operation and thus are often modeled as linear periodically time varying (LPTV) systems. As well known, a linear time varying system can be completely described by the time varying impulse response $h(t,\tau)$. However, in order to fully exploit the periodicity and to contribute to design insight, LPTV systems are usually analyzed

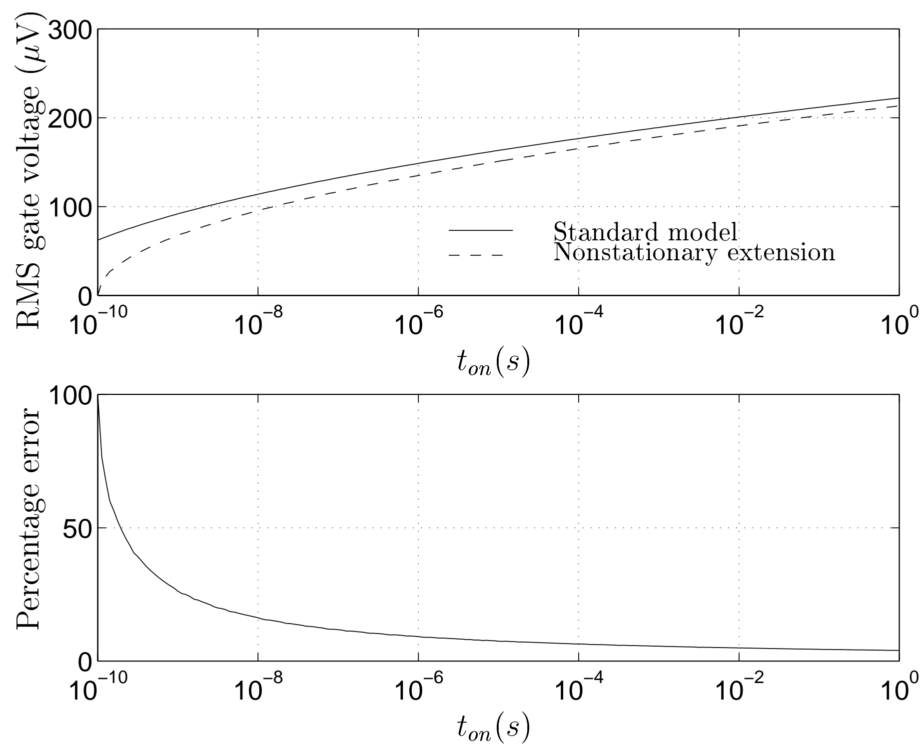

Figure 5.4: RMS gate voltage of an nMOS transistor with $1\mu m^2$ channel area (top) and the percentage error using the standard model (bottom).

in frequency domain. According to the generalized Wiener-Khintchine theorem [29], Fourier transform of $h(t, \tau)$ with regards to τ results in the periodically time varying system transfer function $H(t, f)$. $H(t, f)$ is then expanded using Fourier series representation, leading to the harmonic transfer functions [47]. Using this approach, It becomes obvious that an input signal at certain frequency could cause an output signal that have different frequency content, which is in contrary to the behavior of linear time invariant circuits. The statistics of noise in periodically switched circuits is also vary periodically in time, leading to certain important effects such as up and down conversion of noise spectra. A good such example is given in [41], dealing with time varying shot noise.

In this section we use our nonstationary 1/f noise model to analyze the simplest example of such circuits, a periodically switched transistor. Figure 5.5 depicts a typical setup for measuring 1/f noise psd for a transistor. In the periodically switched case the gate of the transistor is driven by a square wave voltage source that switched between 0V and v_H, which is high enough to bias the transistor in the saturation region. Measured 1/f noise psd using this setup was reported in [1, 6, 15]. These papers comment on the fact that the measured psd is significantly lower than the psd estimated using the standard 1/f model. We now show that our nonstationary model can be used to obtain results that are more consistent with these measurements.

We begin by considering a single active trap. To simplify the analysis, we assume that when the transistor is off, the trap is empty. Using equation 5.10, we can write the autocovariance function of the trapped electron number as

$$\mathcal{C}_\lambda(t, \tau) = \begin{cases} \frac{1}{4} e^{-2\lambda\tau}(1 - e^{-4\lambda(t-nT)}) & nT \le t, t+\tau \le nT + \frac{T}{2} \\ 0 & \text{otherwise} \end{cases} \tag{5.12}$$

Note that $\mathcal{C}_\lambda(t, \tau)$ is periodic in t, and that the trapped electron number is a wide sense cyclostationary process. As proved in [47, 21, 41], low pass filtering or band pass filtering of a wide sense cyclostationary process results in a wide sense stationary process when the filter bandwidth is less than half the switching frequency $\frac{1}{T}$. Spectrum analyzers normally perform this conversion before the spectrum is determined. Therefore the autocovariance of the resulting stationary process can be obtained by

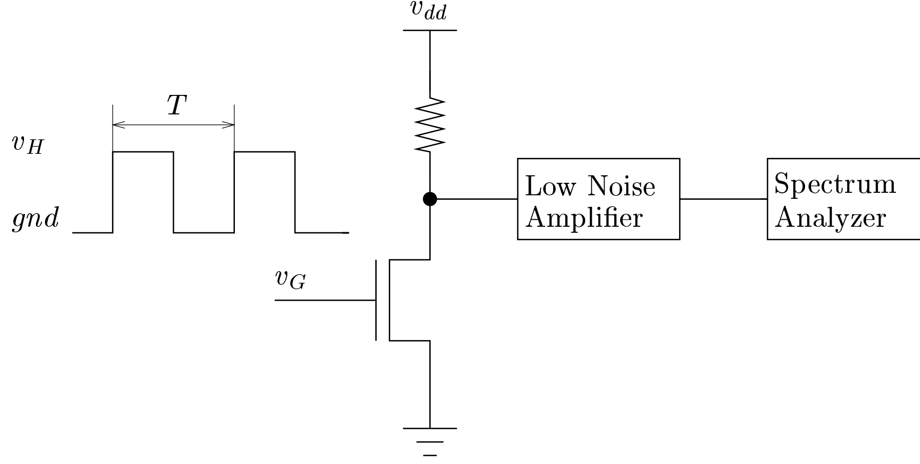

Figure 5.5: Spectrum analysis of a periodically switched nMOS transistor.

averaging the time varying autocovariance over one cycle to get

$$\mathcal{C}^s_\lambda(\tau) = \frac{1}{T}\int_0^T \mathcal{C}_\lambda(t,\tau)dt = (\frac{1}{2} - \frac{1-e^{-2\lambda T}}{4\lambda T})\frac{1}{4}e^{-2\lambda\tau}. \tag{5.13}$$

Note that the standard 1/f noise model gives $\mathcal{C}^s_\lambda(\tau) = \frac{1}{2}\frac{1}{4}e^{-2\lambda\tau}$, and thus predicts the psd curve to be 3dB lower at all frequencies than a dc biased transistor.

Now performing Fourier transform on $\mathcal{C}^s_\lambda(\tau)$, and summing over the contributions of all active traps, we get drain 1/f noise voltage psd

$$S_{V_d}(f) = \xi_V S(f) = \xi_V \int_{\lambda_L}^{\lambda_H} g(\lambda)(\frac{1}{2} - \frac{1-e^{-2\lambda T}}{4\lambda T})\frac{1}{4}\frac{\lambda}{\lambda^2+(\pi f)^2}d\lambda, \tag{5.14}$$

where ξ_V relates the trapped electron number psd to the drain noise voltage psd.

Figure 5.6 plots the simulated drain 1/f noise voltage psd for both the standard and the nonstationary 1/f noise models assuming switching frequency of 2MHz. For comparison we also plot the drain 1/f noise voltage psd for the dc biased transistor. Note that for f much higher than the switching frequency, the two models yield the same result, which, as pointed out is 3dB lower than the noise psd in the dc biased case. For f lower than switching frequency, the two models deviate significantly.

The standard model still predicts noise psd to be 3dB lower than the dc biased case, while the nonstationary model predicts further noise psd reduction that increases as f decreases, which is consistent with the behavior of the measured psd.

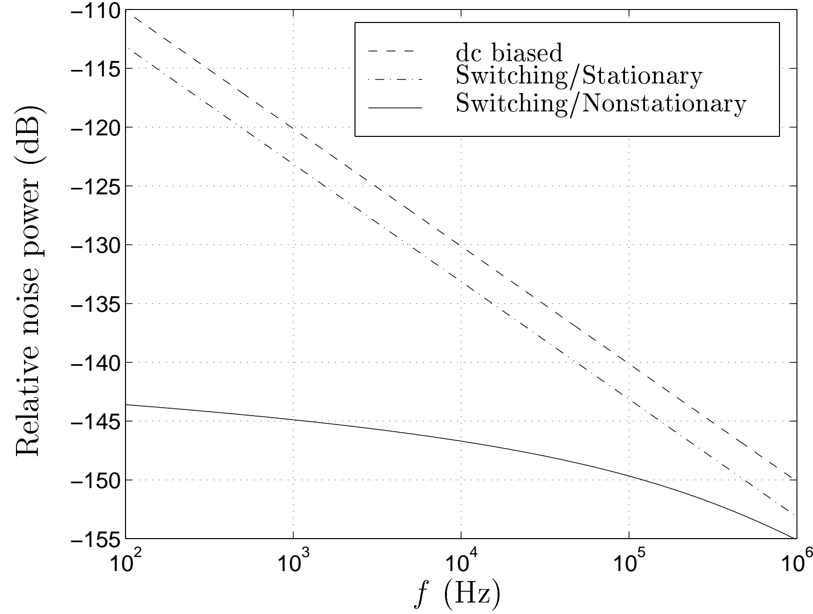

Figure 5.6: Simulated 1/f noise psd for switched and dc biased transistors.

5.5 1/f-induced Phase Noise in a Ring Oscillator

Phase noise in CMOS oscillators have recently been receiving much attention [18, 17, 40] since it sets a limit on the available channel number in wireless communication. It is typically represented by sideband noise power spectral density

$$\mathcal{L}(\Delta\omega) = 10 \log \frac{\mathcal{P}(\omega_0 + \Delta\omega, 1Hz)}{\mathcal{P}(\omega_0)},$$

where $\mathcal{P}(\omega_0 + \Delta\omega, 1Hz)$ represents the sideband power at frequency offset of $\Delta\omega$ from the carrier frequency with a measurement bandwidth of 1Hz. Computing this number requires knowledge of how the device noise current is converted into oscillator output

voltage. In [17] this is done in two steps. The first step involves the conversion of excess injected current into excess phase, which is done via a linear time varying system (LTVS). The second step is phase modulation, where the excess phase is converted into voltage. The LTVS is characterized by its impulse response

$$h(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau),$$

where q_{max} is the maximum charge displacement, u is the unit step function, and Γ is the periodic impulse sensitivity function (ISF). Expanding

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n),$$

and assuming excess injected current due to 1/f noise with psd $\frac{\pi k_F}{C_{ox} A \Delta\omega}$, it can be shown that

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{c_0^2 \pi k_F}{4q_{max}^2 C_{ox} A} \frac{1}{\Delta\omega^3}\right) \tag{5.15}$$

Thus the low frequency noise power gets upconverted to the sideband noise power, which is usually at very high frequency. Note that its power is falling as $\frac{1}{\Delta\omega^3}$ here.

This approach, however, cannot be used to explain the abnormal reduction in phase noise when the transistors in a ring oscillator are periodically turned on and off [15]. We now show that using our nonstationary 1/f noise model, we can explain this reduction. To simplify the derivation, we consider the case where one of the transistors has a much smaller area than the others, and thus its 1/f-induced phase noise dominates. To study the noise due to this transistor, we first consider the case where there is only one active trap. Using the periodic autocovariance function of the trapped electron number as expressed in equation 5.12, we can find the time varying psd [29]

$$S(t,f) = \begin{cases} \frac{1}{4}\frac{\lambda}{\lambda^2+(\pi f)^2}(1-e^{-4\lambda(t-nT)}) & nT \le t, t+\tau \le nT + \frac{T}{2} \\ 0 & \text{otherwise} \end{cases} \tag{5.16}$$

Note that $S(t, f)$ can be seperated as $S(f)\alpha(t)$, where $S(f) = \frac{1}{4}\frac{\lambda}{\lambda^2+(\pi f)^2}$ and $\alpha(t)$ is the remaining periodic function. For this class of cyclostationary noise sources, it is shown [17] that phase noise can still be calculated using equation 5.15, with $S(f)$ representing the noise source, and c_0 computed using $\Gamma_{eff}(t) = \Gamma(t)\alpha(t)$ as the new ISF. In [17] it is also shown that for independent noise sources the total phase noise is simply the sum of the phase noise due to each source. We can use this fact to find the 1/f-induced phase noise psd in the case of many traps, since their trapped electron numbers are independent.

To demonstrate that our nonstationary 1/f noise model can be used to explain the reduction in phase noise consider a ring oscillator with the ISF shown in Figure 5.7. The figure also plots the gate voltage for the transistor under consideration. Figure 5.8 plots the simulated phase noise psd using both the nonstationary and the standard 1/f noise models at 2MHz switching frequency. We also plot the phase noise psd of a non-switching ring oscillator, where the transistor is always on. As can be seen, the standard 1/f noise model reports phase noise that is 6dBc lower than the non-switching case, for all frequencies. The 6dBc reduction, however, is too small when compared to the reported measurements [15], which show over 10dBc reduction in the 1-10kHz range. By comparison, the plot using our nonstationary model shows 10-20dBc reduction in this frequency range. The reduction is caused by the decrease in 1/f noise due to the switching of the transistor as discussed in the previous section. Note that our model predicts an increase in 1/f-induced phase noise above 100kHz relative to the estimates of the stationary model. This we believe is due to the nonflat shape of the $\alpha(t)$ as shown in Figure 5.7, which can cause significant asymmetry in the effective ISF, and thus can increase phase noise.

5.6 Summary

We described a nonstationary extension to the standard 1/f noise model. The model is based on the fact that the active traps are mostly empty when the MOSFET is off. By modifying the RTS model for a single trap to reflect this fact, the noise autocovariance function can be numerically evaluated. We then used our nonstationary extension of

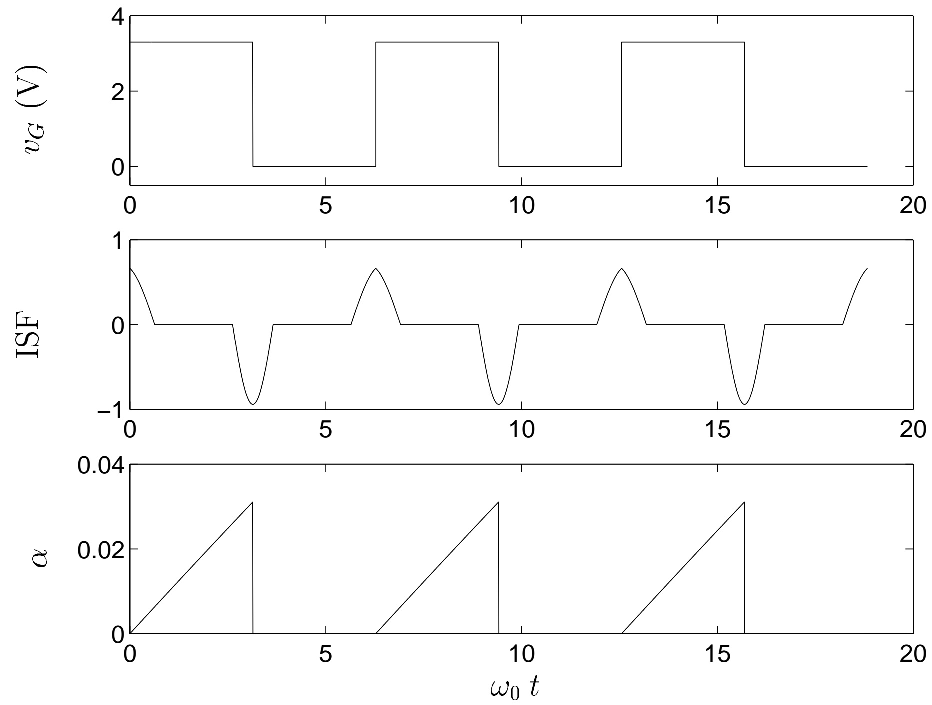

Figure 5.7: The gate voltage of the dominant nMOS transistor in a ring oscillator (top), the associated ISF (middle), and $\alpha(t)$ for $\lambda = 31.6$kHz (bottom).

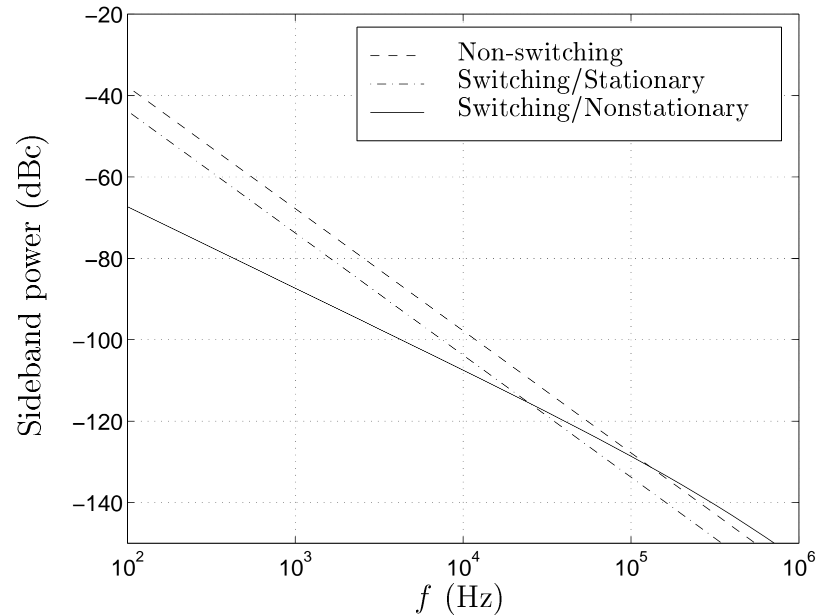

Figure 5.8: Simulated 1/f-induced phase noise psd for a ring oscillator.

the standard 1/f noise model to analyze the effect of 1/f noise in the switched circuit examples, namely the periodically switched transistor and the ring oscillator. In both cases we obtained results that are more consistent with reported measurements than those obtained using the standard 1/f noise model. This not only validates our model but also means that accurate estimates of the effect of 1/f noise on MOSFET circuits can now be obtained for a wider range of applications.

Chapter 6

Analysis of 1/f Noise in CMOS APS

6.1 Introduction

1/f noise in image sensors has been under study for many years [43, 26]. Because 1/f noise is concentrated in low frequency range, human eye is particularly sensitive to its effect. To estimate the noise power due to 1/f noise in a CMOS APS, frequency domain analysis is typically performed using the standard 1/f noise model. A low cutoff frequency f_L that is inversely proportional to the circuit on-time is typically used to get reasonable noise power estimates. The choice of this low cutoff frequency is quite arbitrary, however, and can cause significant inaccuracy in estimating noise power. Moreover, during reset the circuit is not in steady state and thus frequency domain analysis is inappropriate.

To more accurately estimate 1/f noise in CMOS APS, we use the time domain analysis methods developed in chapter 3 and the nonstationary 1/f noise model derived in chapter 5 to perform the noise analysis. We again use the photodiode APS circuit as an example, which is shown in Figure 2.14. For simplicity, we will first find the 1/f noise RMS value at node Bitline in volts. To compute this value, we consider the 1/f noise generated during each step of the APS operation, *i.e.*, during reset, integration, and readout. Once the Bitline referred 1/f noise is determined, it

is straightforward to get the input referred or output referred 1/f noise power using the corresponding circuit transfer functions.

During reset, the 1/f noise is caused by the reset transistor. This transistor is working most of the time in subthreshold and has time varying small signal circuit model. During integration, the 1/f noise is primarily generated by the photodiode. It is due to surface recombination of carriers, and the fluctuation in bulk carrier mobility [44]. For a reverse biased photodiode, the 1/f noise is not directly related to the total current. Instead, it is a function of the dark current, and is typically much smaller than the dark current shot noise, and can thus be ignored. During readout, 1/f noise is mainly due to the pixel level transistors, including follower transistor and access transistor. Column and chip level transistors also cause 1/f noise, which however can be easily reduced to negligible level by simply increasing the transistor area.

The rest of the chapter is organized as follows. In section 6.2 we analyze the 1/f noise due to the follower and the access transistors using time domain analysis and our nonstationary 1/f noise model. We find that the results are approximately twice as large as the results obtained using frequency domain analysis assuming normal readout speed. In section 6.3 we analyze the 1/f noise due to the reset transistor. Here we use the subthreshold time varying circuit model in addition to our nonstationary noise model. We find that the conventional frequency domain results are very inconsistent and very inaccurate: over a factor of 11 lower than time domain analysis in some cases. We isolate the effect of noise model and find that nonstationary noise model produces results that are more consistent with experiments that the standard model does.

6.2 1/f Noise Due to the Follower and Access Transistors

During readout, the 1/f noise is mainly due to the source follower transistor M2, and the access transistor M3. Depicted in Figure 6.1 is the small signal model of the APS

pixel circuit during readout, where $I_{M2}(t)$ and $I_{M3}(t)$ are the 1/f noise current sources associated with M2 and M3, respectively, g_{m2} is the transconductance of M2, g_{d3} is the channel conductance of M3, and C_o is the column storage capacitance.

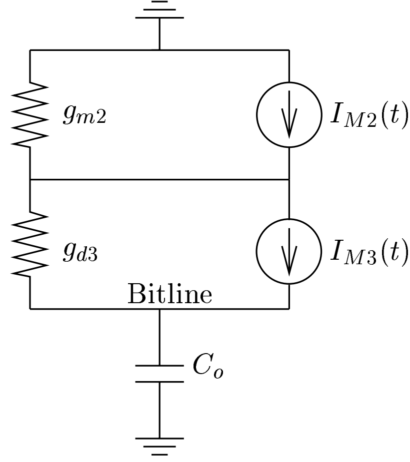

Figure 6.1: Small signal model for 1/f noise analysis during readout.

Let $C_{M2} = (1 + \frac{g_{m2}}{g_{d3}})C_o$ and $C_{M3} = (1 + \frac{g_{d3}}{g_{m2}})C_o$, we get the Bitline voltage due to the noise current sources

$$V_{M2}(t) = \frac{e^{-\frac{g_{m2}}{C_{M2}}t}}{C_{M2}} \int_0^t I_{M2}(s) e^{\frac{g_{m2}}{C_{M2}}s} ds, \tag{6.1}$$

and

$$V_{M3}(t) = \frac{e^{-\frac{g_{d3}}{C_{M3}}t}}{C_{M3}} \int_0^t I_{M3}(s) e^{\frac{g_{d3}}{C_{M3}}s} ds. \tag{6.2}$$

Therefore, the mean square 1/f noise voltage due to each source is given by

$$\overline{V_{M2}^2(t)} = (\frac{q g_{m2}}{A C_{ox}})^2 \frac{e^{-\frac{2 g_{m2}}{C_{M2}}t}}{C_{M2}^2} \int_0^t \int_0^t \int_{\lambda_L}^{\lambda_H} g(\lambda) \mathcal{C}_\lambda(s_1, |s_2 - s_1|) e^{\frac{g_{m2}}{C_{M2}}(s_1+s_2)} d\lambda ds_1 ds_2, \tag{6.3}$$

and

$$\overline{V_{M3}^2(t)} = (\frac{qg_{m3}}{AC_{ox}})^2 \frac{e^{-\frac{2g_{d3}}{C_{M3}}t}}{C_{M3}^2} \int_0^t \int_0^t \int_{\lambda_L}^{\lambda_H} g(\lambda)\mathcal{C}_\lambda(s_1, |s_2 - s_1|) e^{\frac{g_{d3}}{C_{M3}}(s_1+s_2)} d\lambda ds_1 ds_2. \quad (6.4)$$

As a numerical example, we assume that the nMOS transistor mobility is $\mu = 550\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, the bias current is $i_d = 1.8\mu\text{A}$, the reverse bias voltage on the photodiode is $v_{pd} = 1.8\text{V}$, and the threshold voltage is $v_{th} = 0.9\text{V}$ (with body effect). The transconductance of M2 thus is

$$g_{m2} \approx \sqrt{2 i_d \mu C_{ox} W/L} = 4.4 \times 10^{-5}\Omega^{-1}.$$

Since M3 is operating in the linear region and the voltage difference between its drain and source is very small, we can write

$$g_{d3} \approx \mu C_{ox} W/L(v_{G3} - v_{D3} - v_{th}), \quad (6.5)$$

where $v_{G3} = 3.3\text{V}$ is the gate voltage of M3. Note that

$$v_{D3} = v_{pd} - \sqrt{\frac{2i_d}{\mu C_{ox} W/L}} - v_{th}.$$

Substituting into equation 6.5, we get that $g_{d3} = 8.7 \times 10^{-4}\Omega^{-1}$. Consequently the transconductance of M3

$$g_{m3} \approx \frac{i_d}{v_{G3} - v_{S3} - v_{th}} = 1.1 \times 10^{-6}\Omega^{-1}.$$

Now we can numerically evaluate equations 6.3 and 6.4 to find the Bitline RMS noise voltages due to M2 and M3, as functions of the pixel readout time t_{read}. The results are plotted in Figure 6.2 and Figure 6.3, together with the RMS 1/f noise voltages calculated using the frequency domain method. Assuming the pixel readout time of 1μs, the RMS 1/f noise voltage is about 63μV due to follower transistor, and below 1μV due to access transistor. They are twice as large as the values obtained using frequency domain method. The difference between the results computed using

the nonstationary model and the stationary model, as expected, is decreasing as t_{read} gets larger. This is because the traps are approaching their steady states. Also plotted in the figure are the noise voltages due to thermal noise. Note that RMS 1/f noise voltage is higher than thermal noise voltage for the follower transistor, but much lower than thermal noise voltage for the access transistor. The reason for this different behavior is that the follower transistor is working in saturation regime, while the access transistor is working in linear regime. In saturation regime, both thermal and 1/f noise is proportional to the transconductance. In linear regime, 1/f noise is still proportional to the transconductance, while thermal noise is proportional to the channel conductance, which can be much higher than the transconductance.

There is another importance fact that worth pointing out. It is well known that by increasing the storage capacitance C_o the output thermal noise power can be effectively reduced, because the readout circuit bandwidth is reduced. Increasing C_o or reducing bandwidth, however, has no observable effects on the output 1/f noise power. Since 1/f noise energy is concentrated in low frequency range, the reduction of bandwidth cannot be used to effectively reduce 1/f noise power.

6.3 1/f Noise Due to the Reset Transistor

During reset, the 1/f noise is mainly due to the reset transistor. The source follower reset circuit is not only used in the pixel circuit of a CMOS APS, it is also commonly used in the output stage of a CCD image sensor. As depicted in Figure 6.4 during reset, the gate of the transistor is set to a high voltage v_{reset} for a short period of time t_r. To find the output noise power due to the transistor 1/f noise, frequency domain analysis is typically performed using the standard 1/f noise model to get

$$\overline{V_{out}^2(t_r)} = 2\int_{\frac{1}{t_r}}^{\infty} \frac{S_{I_d}(f)}{g_m^2(t_r) + 4\pi^2 f^2 C^2} df,$$

where g_m is the transistor transconductance, and S_{I_d} is the transistor drain current 1/f noise psd. The choice of $\frac{1}{t_r}$ as a low cutoff frequency is quite arbitrary, however. Moreover the circuit is not is steady state [51] and thus it is inappropriate to use

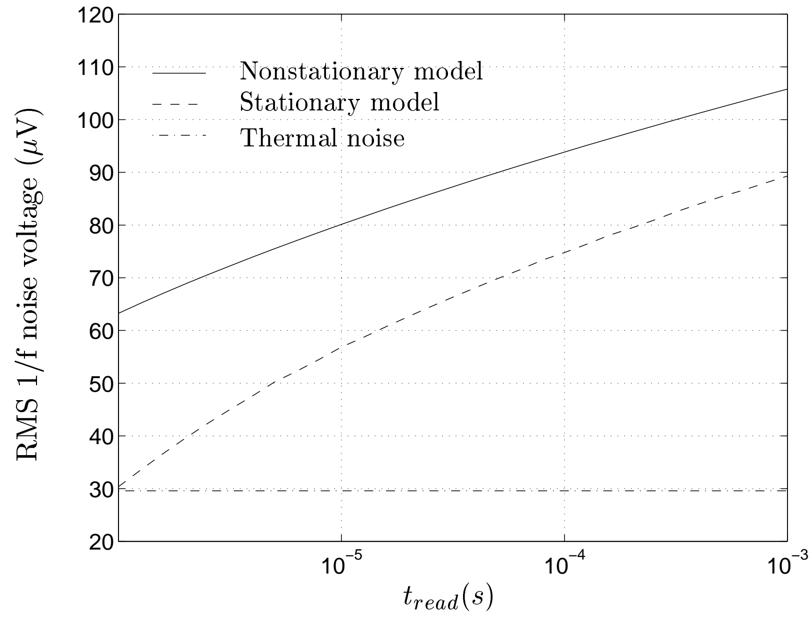

Figure 6.2: Bitline RMS 1/f noise voltage due to the follower transistor.

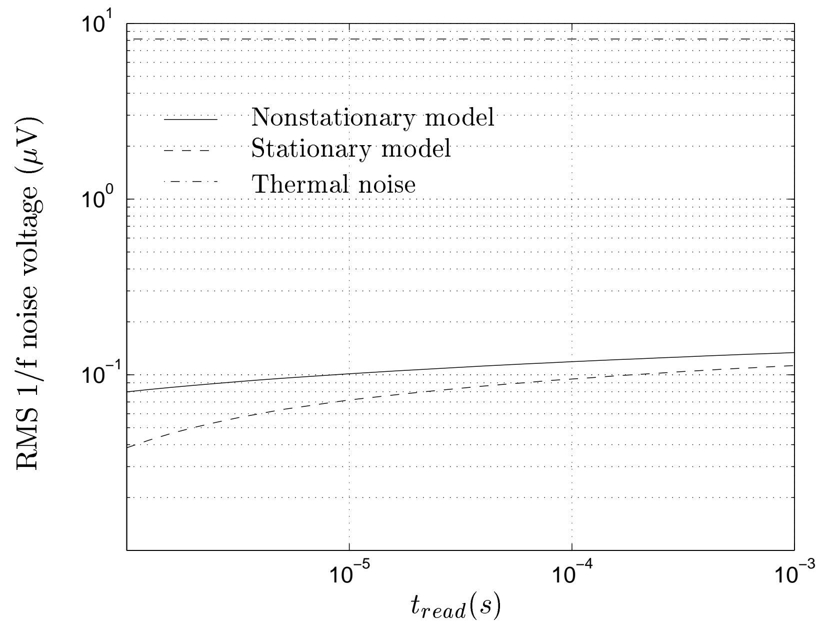

Figure 6.3: Bitline RMS 1/f noise voltage due to the access transistor.

frequency domain analysis.

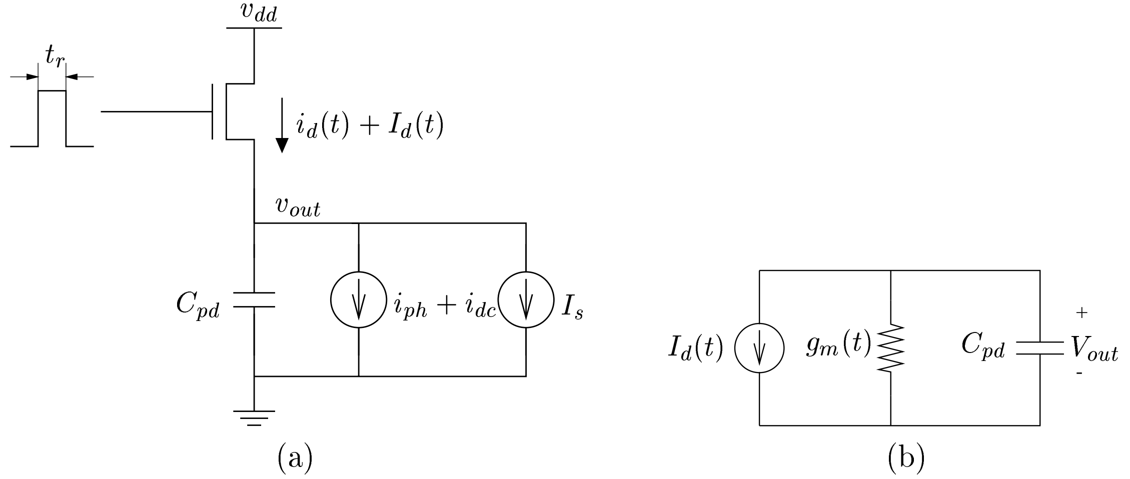

Figure 6.4: CMOS APS circuit during reset (a), and the corresponding small signal model for 1/f noise analysis (b).

In this section we use our nonstationary 1/f noise model and time domain analysis to obtain more accurate noise power estimates. First note that at the beginning of reset, the transistor is either operating in the saturation region or in subthreshold depending on the value of v_{out}. Even if the transistor is first in in saturation, it quickly goes into subthreshold and does not reach steady state. This was explained in detail in chapter 3, where we analyzed reset noise due to thermal and shot noise sources. The circuit noise model during reset is shown in Figure 6.4 (b). The current source $I_d(t)$ models the transistor 1/f noise and g_m is the transistor transconductance in subthreshold, which is time varying. The output noise voltage at the end of reset is given by

$$V_{out}(t_r) = \int_0^{t_r} \frac{I_d(s)}{C} e^{-\int_s^{t_r} \frac{g_m(\tau)}{C} d\tau} ds, \tag{6.6}$$

The output reset noise power is thus given by

$$\overline{V_{out}^2(t_r)} = \left(\frac{q}{AC_{ox}C}\right)^2 \int_0^{t_r} \int_0^{t_r} g_m(s_1) g_m(s_2) \mathcal{C}(s_1, |s_2 - s_1|)$$

$$e^{-\frac{1}{C}\int_{s_1}^{t_r} g_m(\tau_1)d\tau_1} e^{-\frac{1}{C}\int_{s_2}^{t_r} g_m(\tau_2)d\tau_2} ds_1 ds_2. \qquad (6.7)$$

Using the MOS transistor subthreshold I–V characteristics, we get that $g_m(\tau) \approx \frac{C}{\tau+\delta}$, where δ is the thermal time. Thus

$$e^{-\frac{1}{C}\int_{s}^{t_r} g_r(\tau)d\tau} \approx \frac{s+\delta}{t_r+\delta}.$$

Substituting this and equation 5.1 and 5.10 into equation 6.7, we get that

$$\overline{V_{out}^2(t_r)} = (\frac{q}{AC_{ox}})^2 \frac{1}{(t_r+\delta)^2} \int_0^{t_r}\int_0^{t_r}\int_{\lambda_L}^{\lambda_H} \mathcal{C}_\lambda(s_1, |s_2 - s_1|) g(\lambda) d\lambda ds_1 ds_2. \qquad (6.8)$$

Note that this result is virtually independent of the capacitance. This of course is very different from the famous kT/C reset noise due to thermal and shot noise sources. The reason again is that 1/f noise power is concentrated on low frequencies, and thus is less sensitive to circuit bandwidth and hence C.

In Figure 6.5 we compare the results using our method to the results using conventional frequency domain analysis. To perform the frequency domain analysis we need to decide on the value of g_m to use. In that figure we plot the results of the frequency domain analysis for two values of g_m, one at the beginning and the other at the end of the reset time. Note the enormous difference between the curves for the two g_m values. Depending on which g_m value is used, the results can vary from 3.2μV to 68μ V at $t_r = 10\mu$s. This presents yet another serious shortcoming to using frequency domain analysis.

To isolate the effect of using the standard versus the nonstationary noise models, in Figure 6.6 we plot the curves for both models using the same time varying circuit model. In calculating the noise assuming the standard model we simply replace the $\mathcal{C}_\lambda(s_1, |s_2 - s_1|)$ in equation 6.8 by the stationary autocovariance $\mathcal{C}_\lambda(|s_2 - s_1|)$. As can be seen from the two curves, the RMS noise voltage using the standard model is much higher, *e.g.*, 222μV versus 37.2μV at $t_r = 10\mu$s. The noise due to reset transistor shot noise is also plotted and is around 276μV. Note that the RMS 1/f

noise voltage predicted by the standard model is comparable to the effect of the shot noise. Measurement results [51, 42] show however that shot noise dominates the reset noise, which corroborates the analysis using our method.

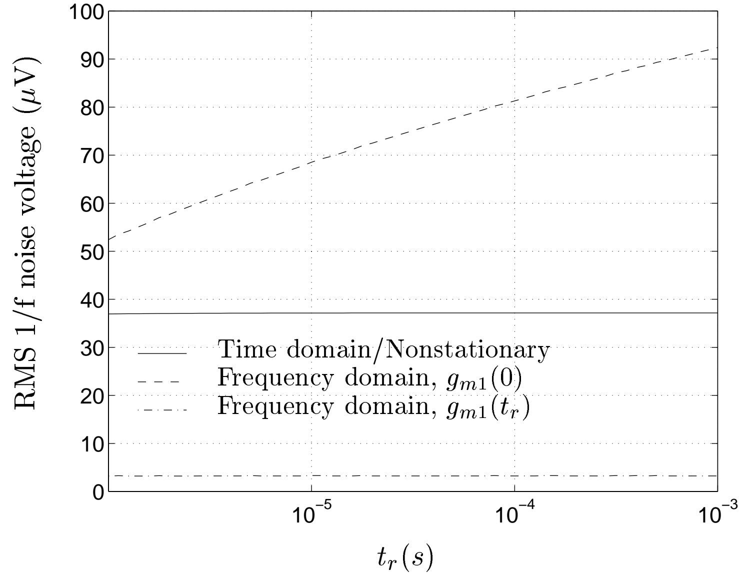

Figure 6.5: Simulated output referred RMS 1/f reset noise using frequency domain analysis versus using the nonstationary extension and time domain analysis.

6.4 Summary

We applied the time domain noise analysis method and the nonstationary 1/f noise model to provide accurate estimates of the effect of 1/f noise due to the pixel level transistors in a CMOS APS. The computed 1/f noise due to the follower and access transistors are found to be approximately twice as large as the results obtained using frequency domain analysis. For the reset transistor, we found that the frequency domain results are very inaccurate. The results depend on some arbitrarily picked circuit parameters, and can be over a factor of 11 lower than time domain analysis in some cases. We also isolate the 1/f noise model effect by performing time domain noise analysis using both stationary and nonstationary 1/f noise models. The results

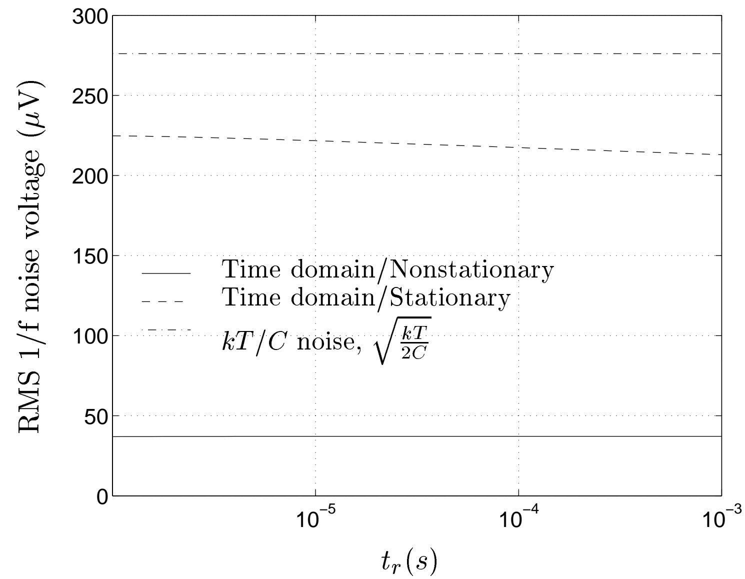

Figure 6.6: Simulated output referred RMS 1/f reset noise using standard 1/f noise model versus using the nonstationary extension, both assuming time varying circuit model.

showed that nonstationary model produced estimates that are more consistent with experiments.

Chapter 7

Conclusion

7.1 Summary

We have presented the first complete and rigorous analysis of temporal noise in CMOS image sensors. It takes the time varying circuit models and nonstationary noise sources into consideration.

Using time domain analysis, instead of the more traditional frequency domain analysis method, we found that the reset noise power due to thermal noise is at most half of its commonly quoted KTC value. This fundamental result was corroborated by several published experimental data including data collected in our lab. The lower reset noise, however, comes at the expense of image lag. We found that alternative reset methods such as overdriving the reset transistor gate or using a pMOS transistor can alleviate lag, but double the reset noise power. We proposed a new reset method that alleviates lag without increasing reset noise. We analyzed noise due to the photodetector shot noise taking nonlinearity into consideration and found that nonlinearity improves SNR at high illumination. We also analyzed noise during readout using both hand analysis and SPICE simulation.

We have developed methods for CMOS image sensors characterization. We characterized the 64×64 CMOS APS test structure fabricated in a 0.35μ standard digital CMOS process. We found that the measured reset noise is indeed very close to the half kT/C result derived in previous chapter. The measured SNR is also consistent

with the calculated shot noise using our nonlinear model. We also demonstrated the incomplete reset induced image lag.

We have proposed a nonstationary extension to the standard 1/f noise model. The model is based on the fact that the active traps are mostly empty when the MOSFET is off. By modifying the RTS model for a single trap to reflect this fact, the noise autocovariance function can be numerically evaluated. We used our nonstationary extension of the standard 1/f noise model to analyze the effect of 1/f noise in the switched circuit examples, namely the periodically switched transistor and the ring oscillator. In both cases we obtained results that are more consistent with reported measurements than those obtained using the standard 1/f noise model. This not only validates our model but also means that accurate estimates of the effect of 1/f noise on MOSFET circuits can now be obtained for a wider range of applications.

We have applied the time domain noise analysis method and the nonstationary 1/f noise model to provide accurate estimates of the effect of 1/f noise due to the pixel level transistors in a CMOS APS. The computed 1/f noise due to the follower and access transistors are found to be approximately twice as large as the results obtained using frequency domain analysis. For the reset transistor, we found that the frequency domain results are very inaccurate. The results depend on some arbitrarily picked circuit parameters, and can be over a factor of 11 lower than time domain analysis in some cases. We also isolate the 1/f noise model effect by performing time domain noise analysis using both stationary and nonstationary 1/f noise models. The results showed that nonstationary model can produce estimates that are more consistent with experiments.

Since temporal noise sets the fundamental limit on image sensor performance, it is very important to be able to accurately estimates the temporal noise power. We believe that the thesis contributes to better understand the noise mechanism and thus leads to further noise suppression. This serves the purpose of improving imaging quality of CMOS image sensors, and making it a superior choice among imaging devices.

7.2 Future Work and Future Directions

In the thesis we analyzed the intrinsic noise, including thermal, shot, and 1/f noise. Other noise sources are generally reducible through judicious design practice. As more functions are integrated onto the same chip that holds the image sensor, it is, however, harder to suppress the noise due to those other noise sources. One such example is the noise coupled into the sensor array from the peripheral circuits through the substrate. When control, memory, and image processing blocks are integrated together with the image sensors which might have over a million pixels, the cross talk between the sensor array and those other function blocks becomes very strong and hard to track. As a result, it is very difficult to identify and suppress the substrate noise. A practical model that can efficiently calculate the substrate noise effect will extend our knowledge of noise behavior in CMOS image sensors, and will greatly benefit the design of the next generation of highly integrated image sensor systems.

While pursuing higher level integration, further image quality improvement is also indispensable for CMOS image sensors. It is crucial to extend the use of CMOS image sensors into high end imaging applications. The thesis focuses on how noise sets a fundamental limit on dynamic range and signal to noise ratio. It would be useful to extend the work to also consider the relationship between noise and other important image sensor parameters. For example, since each pixel has different 1/f noise characteristics, the 1/f noise may appear as different DC offsets among the pixels. As these pixels are independent, the 1/f drift will be different and the pattern will change with time. This time varying "fixed" pattern noise can cause problem for video application. Noise may also change the sensor color response. In a color filter array based CMOS image sensors, the different noise added to different pixels may cause distorted color. Since human observer is more sensitive to the color distortion than to the magnitude variation, it is important to fully understand the effect of temporal noise on color image sensors.

To keep scaling the CMOS image sensors to even smaller pixel size and larger format, without sacrifice the image quality, the requirement of low noise operation becomes more strict. Because the full well electron capacity and quantum efficiency

are generally reduced, the signal is becoming weaker, and thus it is desirable to minimize the noise level. Noise on the other hand, cannot be reduced at will. It would be interesting to find out if noise imposes limits on the sensor scaling. Similar question can be asked for QE, full well electron capacity, and other parameters. Identifying the limiting factor may help us to break the barrier of CMOS image sensor scaling.

Design for testing is another important field that needs improvement. The CMOS image sensors is in general hard to test, because it involves optoelectronic response, mixed signal operation, and has very limited area per pixel. Increased testability will greatly improve the characterization accuracy, and thus help to identify the bottleneck in sensor design. For example, the extra drain voltage line of the reset transistor has been used to test the readout circuit response, which helped to better estimate the sensor sense node capacitance, quantum efficiency, noise, and many other parameters. Improvements of testability, however, must be done without adversely affecting the sensor performance.

The nonstationary 1/f noise model presented in the thesis has been used to analyze switched circuits including CMOS image sensors. It would be interesting to apply the model to analyze other circuits as well. The better understanding of 1/f noise behavior may lead to some novel 1/f noise reduction scheme. The model itself can also be improved, *e.g.*, by refining the modeling of the trap states when the transistor is switched from on to off.

Finally, multiple sampling has been demonstrated to greatly improve image sensor dynamic range by virtually increasing the well capacity. It is worth thinking if multiple sampling can also be applied to efficiently reduce noise floor, thus increasing both dynamic range and sensitivity. One simple algorithm is to average all the samples. By intelligently picking the sampling time one can expect to achieve higher noise reduction.

Bibliography

[1] I. Bloom and Y. Nemirovsky. 1/f Noise Reduction of Metal-Oxide-Semiconductor Transistors by Cycling From Inversion to Accumulation. *Applied Physics Letters*, 58(15):1664–1666, April 1991.

[2] T. Boutchacha, G. Ghibaudo, G. Guegan, and T. Skotnicki. Low Frequency Noise Characterization of 0.18um Si CMOS Transistors. *Microelectron. Reliab.*, 37(10/11):1599–1602, 1997.

[3] P. Centen. CCD On-Chip Amplifiers: Noise Performance versus MOS Transistor Dimensions. *IEEE Trans. Electron Devices*, 38(5):1206–1216, May 1991.

[4] J. Chang, A. A. Abidi, and C. R. Viswanathan. Flicker Noise in CMOS Transistors from Subthreshold to Strong Inversion at Various Temperatures. *IEEE Trans. Electron Device*, 41(11):1965–1971, November 1994.

[5] S. Decker, D. McGrath, K. Brehmer, and C. G. Sodini. A 256 $\times$ 256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column–Parallel Digital Output. *IEEE J. Solid-State Circuits*, 33(12):2081–2091, 1998.

[6] B. Dierickx and E. Simoen. The Decrease of "Random Telegraph Signal" Noise in Metal-Oxide-Semiconductor Field-Effect Transistors When Cycled From Inversion to Accumulation. *J. Applied Physics*, 71(4):2028–2029, February 1992.

[7] A. El Gamal, B. Fowler, H. Min, and X. Liu. Modeling and Estimation of FPN Components in CMOS Image Sensors. In *Proc. SPIE*, volume 3301, pages 168–177, San Jose, CA, Jan. 1998.

[8] R. Forchheimer and A. Odmark. A Single Chip Linear Array Processor, in Applications of digital image processing. *SPIE*, 1983.

[9] R. Forchheimer, P.Ingelhag, and C. Jansson. MAPP2200, a second generation smart optical sensor. *SPIE*, 1992.

[10] E. R. Fossum. Active Pixel Sensors: are CCD's dinosaurs. In *Proceedings of SPIE*, pages 2–14, San Jose, CA, February 1993.

[11] E. R. Fossum. CMOS Image Sensors: Electronic Camera On A Chip. In *Proceedings of International Electron Devices Meeting*, pages 17–25, Washington, DC, December 1995.

[12] B. Fowler, A. El Gamal, D. Yang, and H. Tian. A Method for Estimating Quantum Efficiency for CMOS Image Sensors. In *Proc. SPIE*, volume 3301, pages 178–185, San Jose, CA, Jan. 1998.

[13] B. Fowler, A. El Gamal, and D. X. D. Yang. "A CMOS Area Image Sensor with Pixel-Level A/D Conversion". In *ISSCC Digest of Technical Papers*, San Fransico, CA, February 1994.

[14] B. Fowler, D. Yang, H. Min, and A. El Gamal. Single Pixel Test Structures for Comparative Analysis of CMOS Image Sensors. In *1997 IEEE Work Shop on CCDs and AIS*, Brugge, Belgium, June 1997.

[15] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, E. van Tuijl, and B. Nauta. Intrinsic 1/f Device Noise Reduction and Its Effect on Phase Noise in CMOS Ring Oscillators. *IEEE J. Solid-State Circuits*, 34(7):1022–1025, July 1999.

[16] P.R. Gray and R.G. Meyer. *Analysis and Design of Analog Integrated Circuits.* John Wiley & Sons, Inc., New York, 1993.

[17] A. Hajimiri and T. H. Lee. A General Theory of Phase Noise in Electrical Oscillators. *IEEE J. Solid-State Circuits*, 33(2):179–194, February 1998.

[18] A. Hajimiri, S. Limotyrakis, and T. H. Lee. Jitter and Phase Noise in Ring Oscillators. *IEEE J. Solid-State Circuits*, 34(6):790–804, June 1999.

[19] G. C. Holst. *CCD Arrays Cameras and Displays: second edition.* JCD Publishing, 1998.

[20] C. Hu, G. P. Li, E. Worley, and J. White. Consideration of Low-Frequency Noise in MOSFET's for Analog Performance. *IEEE Electron Device Letters*, 17(12):552–554, December 1996.

[21] C. D. Hull and R. G. Meyer. A Systematic Approach to the Analysis of Noise in Mixers. *IEEE Trans. Circuits Syst.*, 40(12):909–919, December 1993.

[22] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng. A Unified Model for the Flicker Noise in Metal-Oxide-Semiconductor Field-Effect Transistors. *IEEE Trans. Electron Device*, 37(3):654–665, March 1990.

[23] J. Hynecek. Spectral Analysis of Reset Noise Observed in CCD Charge-Detection Circuits. *IEEE Trans. Electron Devices*, 37(3):640–647, Mar. 1990.

[24] C. Jakobson, I. Bloom, and Y. Nemirovsky. 1/f Noise in CMOS Transistors for Analog Applications From Subthreshod to Saturation. *Solid-State Electronics*, 42(10):1807–1817, 1998.

[25] J. Janesick et al. Charge-coupled-device response to electron beam energies of less than 1 keV up to 20 keV. *Optical Engineering*, 26(8):686–91, August 1987.

[26] J. F. Johnson. Methodology for Simulating 1/f Noise Characteristics in the Time Domain for Infrared Focal Plane Applications. In *Proc. the SPIE*, pages 31–37, Orlando, Florida, April 1997.

[27] J. S. Kim, C. H. Park, and H. S. Min adn Y. J. Park. Theory of 1/f Noise Current in n^+p Diodes, n^+p Photodiodes, and Schottky Diodes. In *Quantum 1/f Noise and Other Low Frequency Fluctuations in Electronic Devices: Seventh Symposium*, pages 123–128, 1999.

[28] M. J. Kirton and M. J. Uren. Noise in Solid-State Microstructures: A New Perspective on Individual Defects, Interface States and Low-frequency (1/f) Noise. *Advances in Physics*, 38(4):367–468, 1989.

[29] D. G. Lampard. Generalization of the Wiener-Khintchine Theorem to Nonstationary Processes. *J. Applied Physics*, 25(6):802–803, June 1954.

[30] M. Loinaz, K. Singh, A. Blanksby, D. Inglis, K. Azadet, and B. Ackland. A 200mW 3.3V CMOS color camera IC producing 352x288 24b Video at 30frames/s. In *ISSCC Digest of Technical Papers*, pages 168–169, San Fransisco, CA, February 1998.

[31] C. Mead. *Analog VLSI and Neural Systems*. Addison Wesley, 1989.

[32] S. Mendis et al. Progress in CMOS Active Pixel Image Sensors. In *Proceedings of SPIE*, pages 19–29, San Jose, CA, February 1994.

[33] S. Mendis, E. R. Fossum, et al. A 128×128 CMOS Active Pixel for Highly Integrated Imaging Systems. In *IEEE IEDM Technical Digest*, San Jose, CA, December 1993.

[34] S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, C. O. Staller, Q. Kim, and E. R. Fossum. CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems. *IEEE J. Solid-State Circuits*, 32(2):187–197, 1997.

[35] R.S. Muller and T.I. Kamins. *DEVICE ELECTRONICS FOR INTEGRATED CIRCUITS*. Wiley, 1986.

[36] R. Panicacci et al. 128 Mb/s Multiport CMOS Binary Active-Pixel Image Sensor. In *ISSCC96 Techincal Digest*, February 1996.

[37] P.Denyer, D. Renshaw, G. Wang, and M. Lu. A Single-Chip Video Camera with On-Chip Automatic Exposure Control. In *ISIC-91*, 1991.

[38] P.Denyer, D Renshaw, G. Wang, and M. Lu. CMOS Image Sensors For Multimedia Applications. In *CICC93*, 1993.

[39] P.Denyer, D. Renshaw, G. Wang, M. Lu, and S.Anderson. On-Chip CMOS Sensors for VLSI Imaging Systems. In *VLSI-91*, 1991.

[40] B. Razavi. A Study of Phase Noise in CMOS Oscillators. *IEEE J. Solid-State Circuits*, 31(3):331–343, March 1996.

[41] J. Roychowdhury, D. Long, and P. Feldmann. Cyclostationary Noise Analysis of Large RF Circuits with Multitone Excitations. *IEEE J. Solid-State Circuits*, 33(3):324–336, March 1998.

[42] R. Sarpeshkar, T. Delbruck, and C.A. Mead. White Noise in MOS Transistors and Resistors. *IEEE Circuits and Devices Magazine*, 9(6):23–29, November 1993.

[43] D. A. Scribner, M. R. Kruer, J. C. Gridley, and K. Sarkady. Physical Limitations to Nonuniformity Correction in IR Focal Plane Arrays. In *Proc. the SPIE*, pages 185–202, 1988.

[44] E. Simoen and C. L. Claeys. On the Geometry Dependence of the 1/f Noise in CMOS Compatible Junction Diodes. *IEEE Trans. Electron Device*, 46(8):1725–1732, August 1999.

[45] K. Singh. Noise Analysis of a Fully Integrated CMOS Image Sensor. In *Proc. SPIE*, volume 3650, pages 44–51, San Jose, CA, Jan. 1999.

[46] S. Smith, J. Hurwitz, M. Torrie, D. Baxter, A. Holmes, M. Panaghiston, R. Henderson, A. Murray, S. Anderson, and P. Denyer. A single-chip 306x244-pixel CMOS NTSC video camera. In *ISSCC Digest of Technical Papers*, pages 170–171, San Fransisco, CA, February 1998.

[47] T. Strom and S. Signell. Analysis of Periodically Switched Linear Circuits. *IEEE Trans. Circuits Syst.*, 24(10):531–541, October 1977.

[48] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai. No Image Lag Photodiode Structure in the Interline CCD Image Sensor. *IEDM Tech. Dig.*, pages 324–327, 1982.

[49] A. J. P. Theuwissen. *Solid-State Imaging with Charge-Coupled Devices*. Kluwer Academic Publishers, 1995.

[50] K. K. Thornber. Theory of Noise in Charge-Transfer Devices. *Bell Sys. Tech. J.*, 53(7):1211–1262, Sep. 1974.

[51] H. Tian, B. Fowler, and A. El Gamal. Analysis of Temporal Noise in CMOS APS. In *Proc. SPIE*, volume 3649, pages 177–185, San Jose, CA, Jan. 1999.

[52] S. P. Tobin, S. Iwasa, and T. J. Tredwell. 1/f Noise in (Hg, Cd)Te Photodiodes. *IEEE Trans. Electron Device*, 27(1):43–48, January 1980.

[53] A. van der Ziel. *Noise in Solid State Devices and Circuits*. Wiley, 1986.

[54] L. K. J. Vandamme, X. Li, and D. Rigaud. 1/f Noise in MOS Devices, Mobility or Number Fluctuations? *IEEE Trans. Electron Device*, 41(11):1936–1944, November 1994.

[55] G. Weckler. Operation of p-n junction photodetectors in a photon flux integration mode. *IEEE Journal of Solid State Circuits*, SC-2(3):65–73, 1967.

[56] O. Yadid-Pecht, B. Mansoorian, E. R. Fossum, and B. Pain. Optimization of Noise and Responsivity in CMOS Active Pixel Sensors for Detection of Ultra Low Light Levels. In *Proc. SPIE*, volume 3019, pages 125–136, San Jose, CA, Feb. 1997.

[57] O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, and E. R. Fossum. CMOS Active Pixel Sensor Star Tracker with Regional Electronic Shutter. *IEEE J. Solid-State Circuits*, 32(2):285–288, Feb. 1997.

[58] D. Yang, B. Fowler, and A. El Gamal. A 128×128 CMOS Image Sensor with Multiplexed Pixel Level A/D Conversion. In *CICC96*, 1996.

[59] D. Yang, B. Fowler, A. El Gamal, H. Min, M. Beiley, and K. Cham. Test Structures for Characterization and Comparative Analysis of CMOS Image Sensors. In *Proc. SPIE*, volume 2950, pages 8–17, Berlin, FRG, Oct. 1996.

[60] D.X.D. Yang, A. El Gamal, B. Fowler, and H. Tian. A 640×512 CMOS Image Sensor with Ultra Wide Dynamic Range Floating Point Pixel Level ADC. In *ISSCC Digest of Technical Papers*, San Fransisco, CA, February 1999.