A Nyquist Rate Pixel Level ADC for CMOS Image Sensors

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Outline

- **Motivation and background**
- **Our ADC Operation**
- **Implementation**

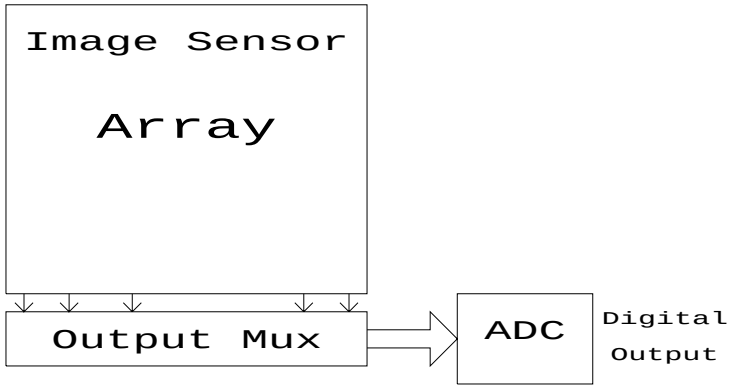
Motivation

Single chip CMOS digital camera

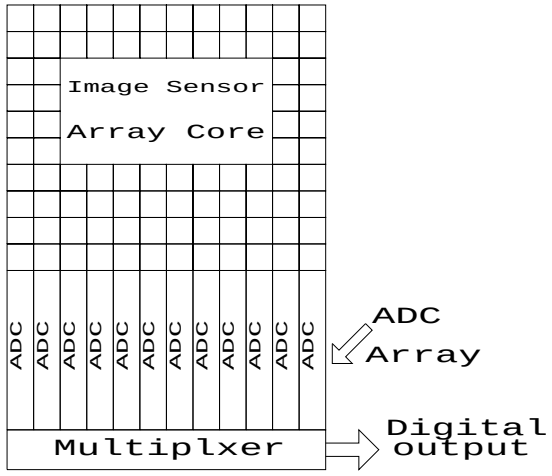
- **Image sensor array (e.g. APS)**
- **ADC**
- **Image processing and compression**
- **Control**
- **Memory**

Approaches to ADC Integration

- Chip Level



- Column Level



Pixel Level ADC

- **ADC close to signal generation always better**
  - **highest SNR**
  - **lowest power**
- **Scalable sensor architecture**
- **Process portability – compatible with digital CMOS**
- **But**
  - **Very limited silicon area** $\approx 10\mu m \times 10\mu m$

Constraints of Pixel Level ADC

- **Cannot use bit-parallel ADCs**
  - **bit-serial is the way to go**
- **Cannot use conventional Nyquist rate bit-serial ADCs (e.g. SA, algorithmic).**
  - **simple and robust circuits are a must**

Pixel Level Sigma Delta ADC

ISSCC 94, CICC 96

- **1-bit first order $\Sigma\Delta$ ADC per pixel or per four pixels, operating simultaneously**
- **Simple imprecise circuits can be used**

Limitations of Sigma Delta ADC

- **Poor low light response**
- **Moderate fixed pattern noise**
- **High output data rate - need decimation**

Multi-channel bit-serial (MCBS) ADC

- Reduces output data rate
- Improves low light response
- Lowers fixed pattern noise
- Provides programmable step size quantization
- Provides in pixel testability

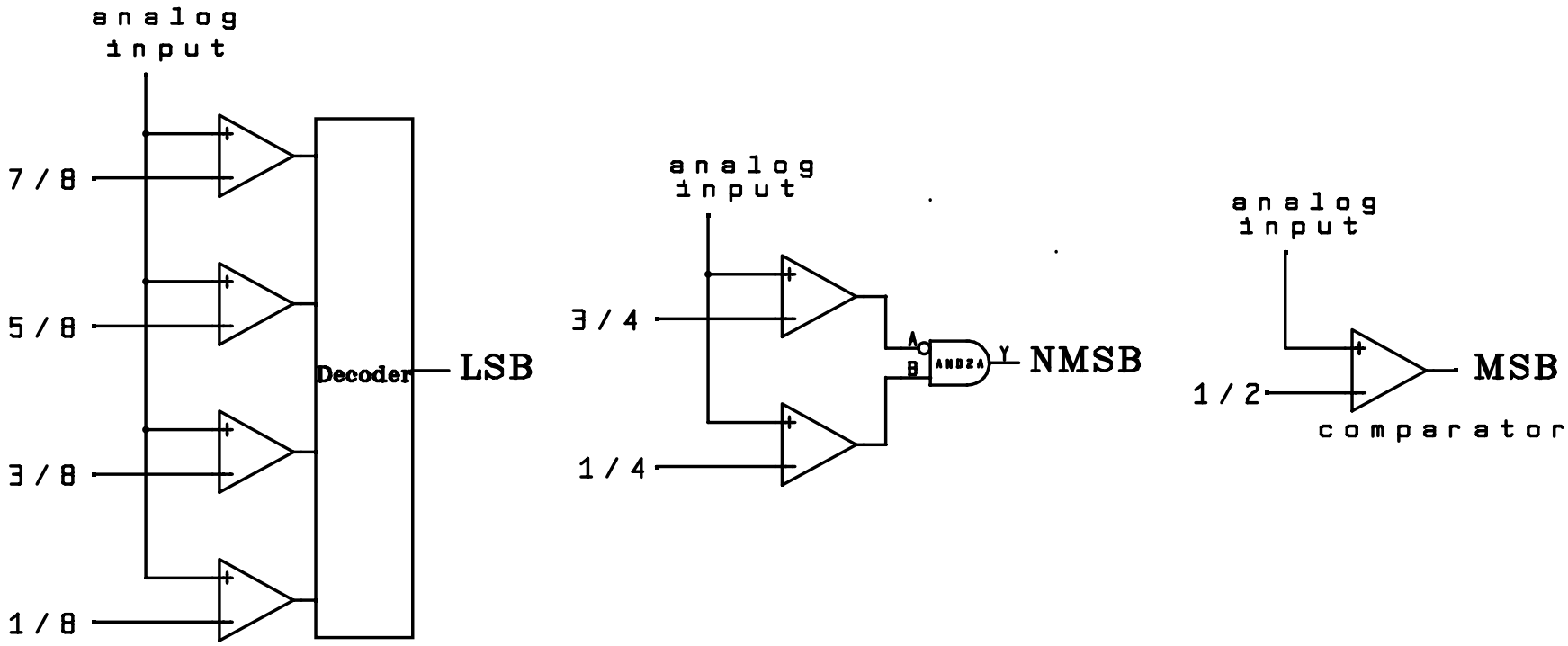
MCBS ADC Method

ADC implements a quantization table

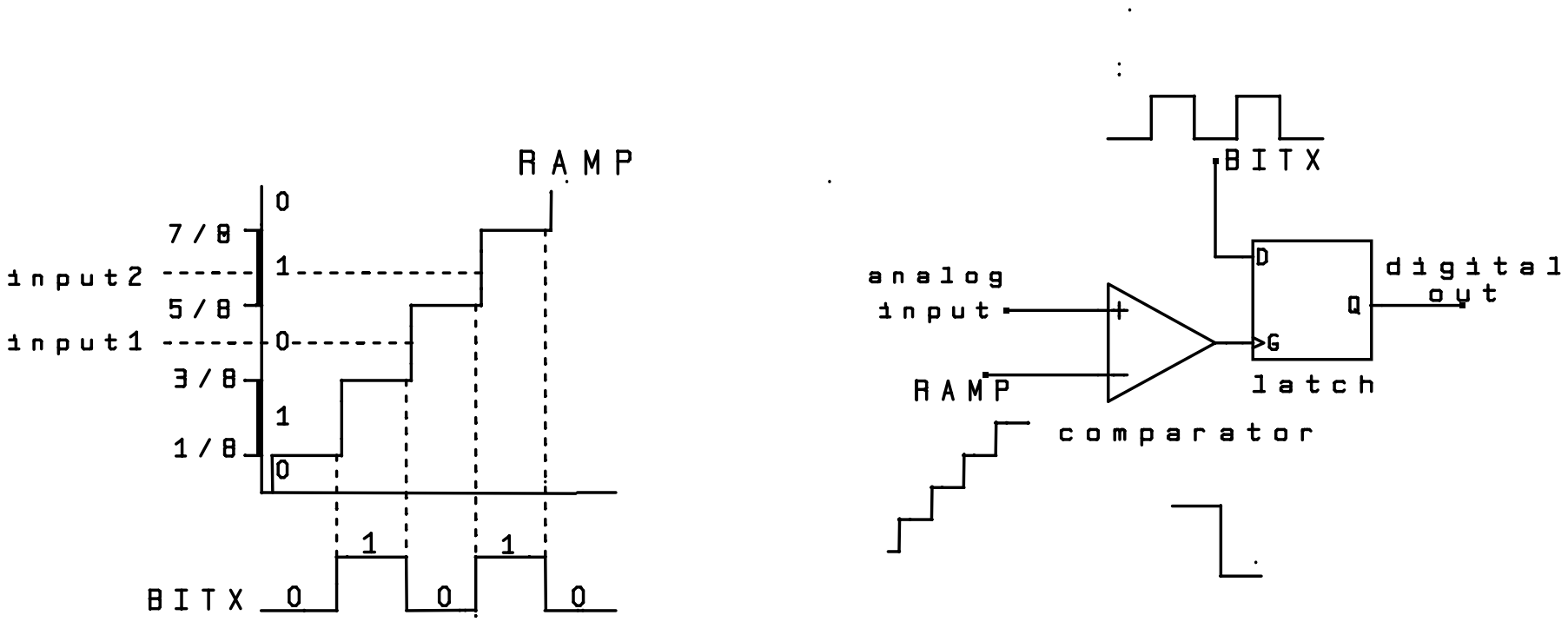
Quantization table	
ADC Input S	Gray Code
$0 - \frac{1}{8}$	0 0 0
$\frac{1}{8} - \frac{2}{8}$	0 0 1
$\frac{2}{8} - \frac{3}{8}$	0 1 1
$\frac{3}{8} - \frac{4}{8}$	0 1 0
$\frac{4}{8} - \frac{5}{8}$	1 1 0
$\frac{5}{8} - \frac{6}{8}$	1 1 1
$\frac{6}{8} - \frac{7}{8}$	1 0 1
$\frac{7}{8} - 1$	1 0 0

Key Point: Each output bit is a binary-valued function (independent of other bits)

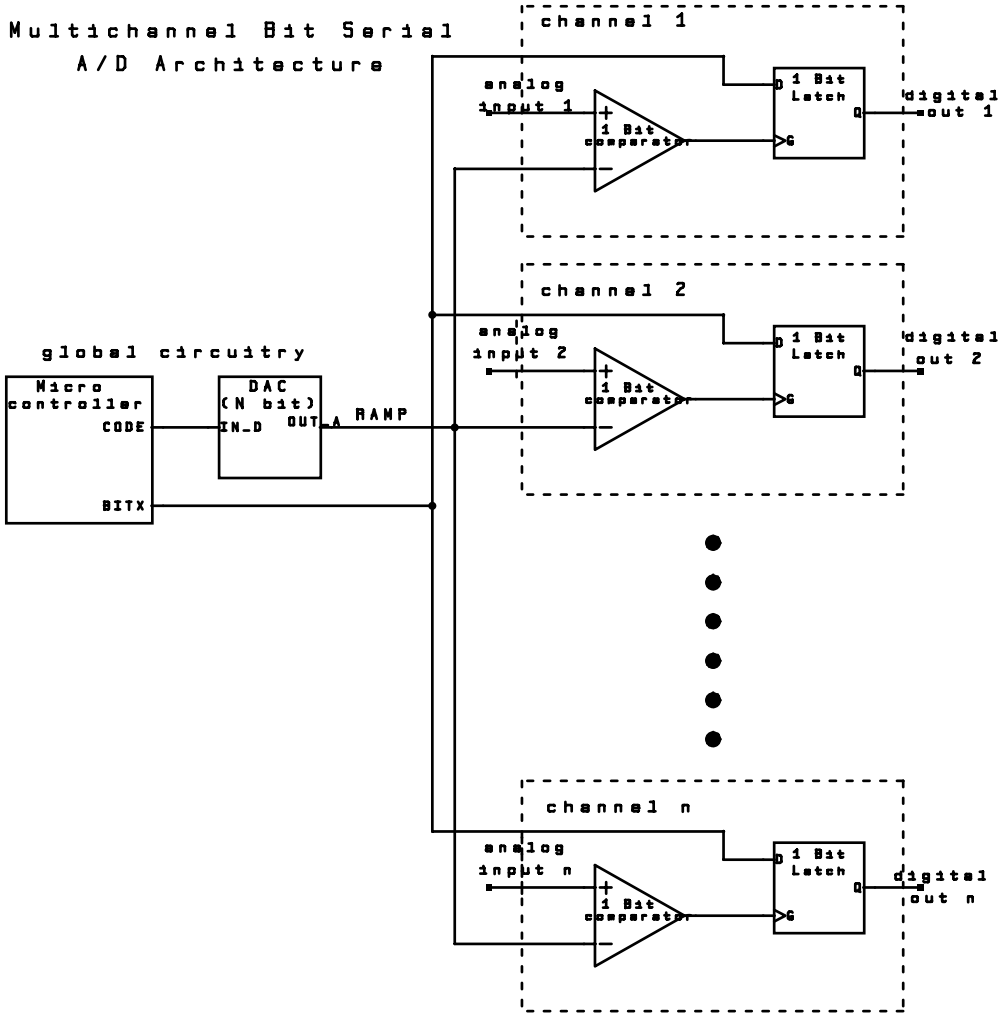
Flash ADC (Not MCBS ADC)



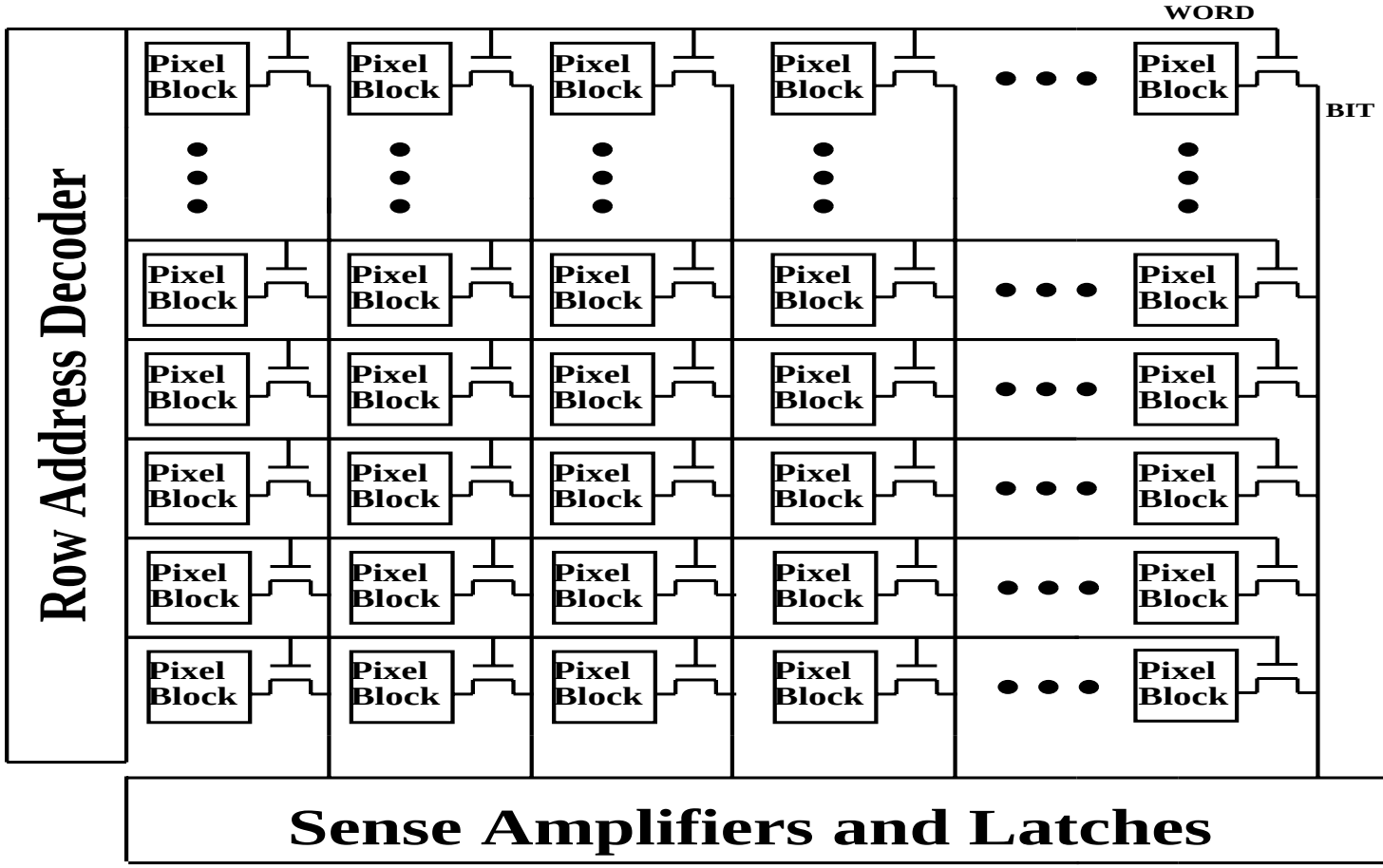
How 1-bit Comparator/Latch Works



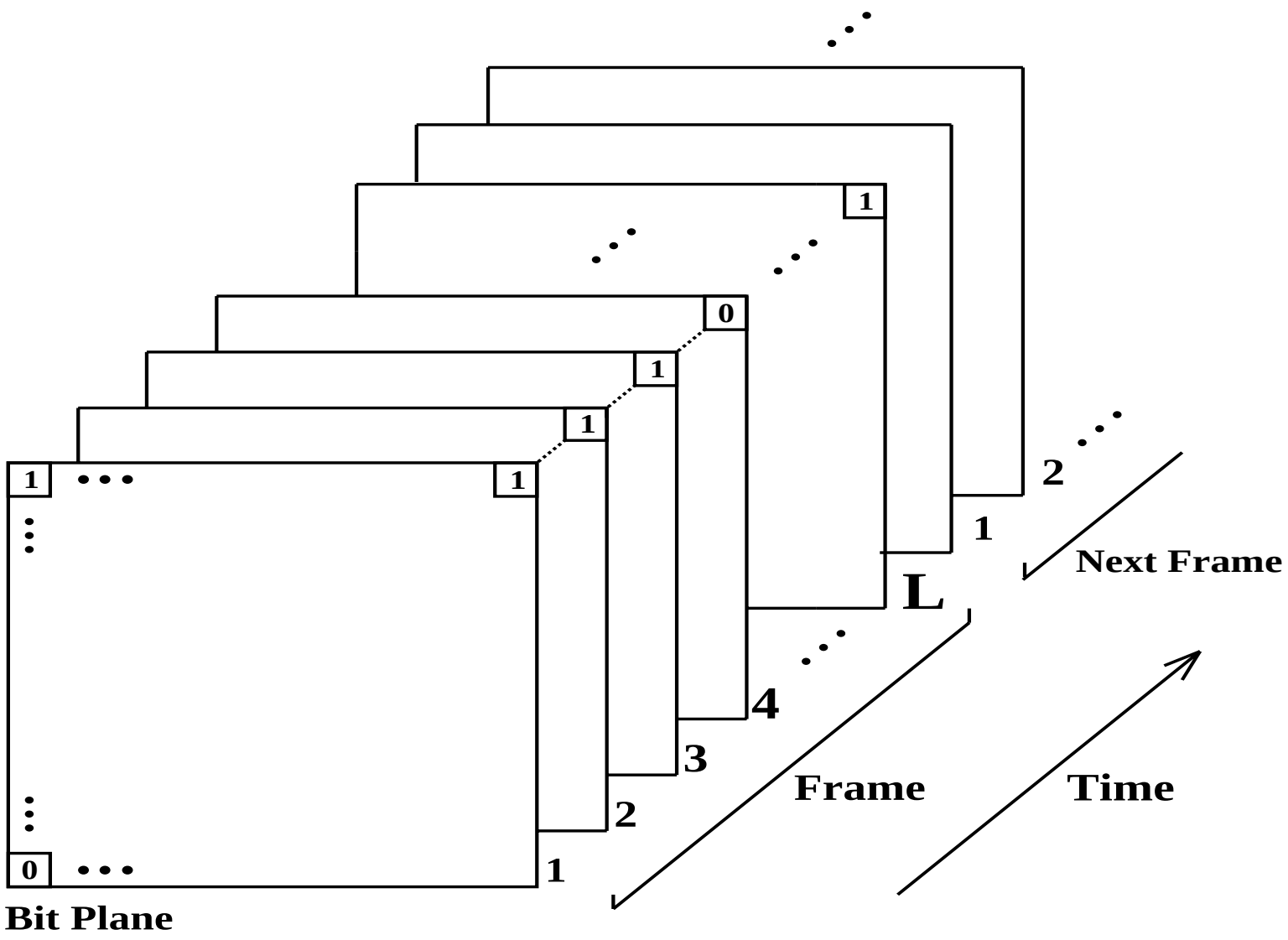
MCBS ADC – Block Diagram



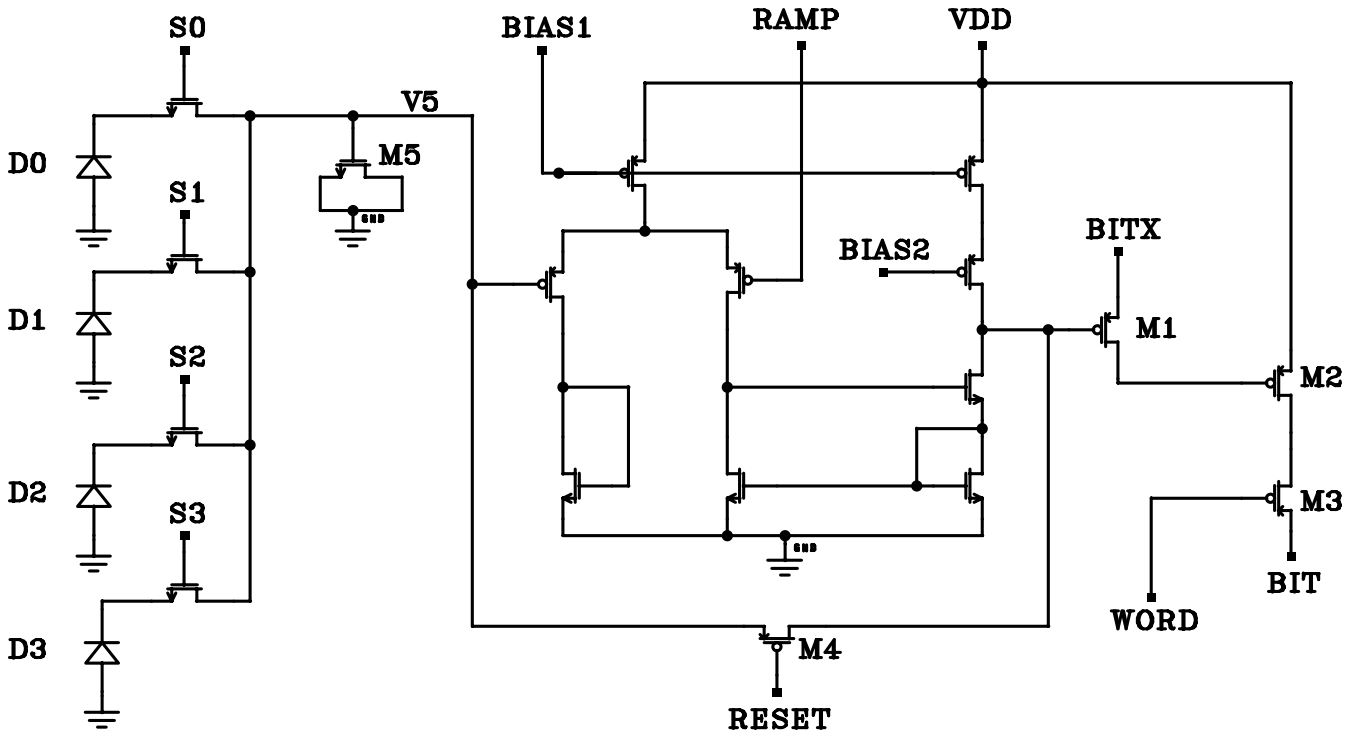
Block Diagram for Image Sensor with Pixel Level ADC



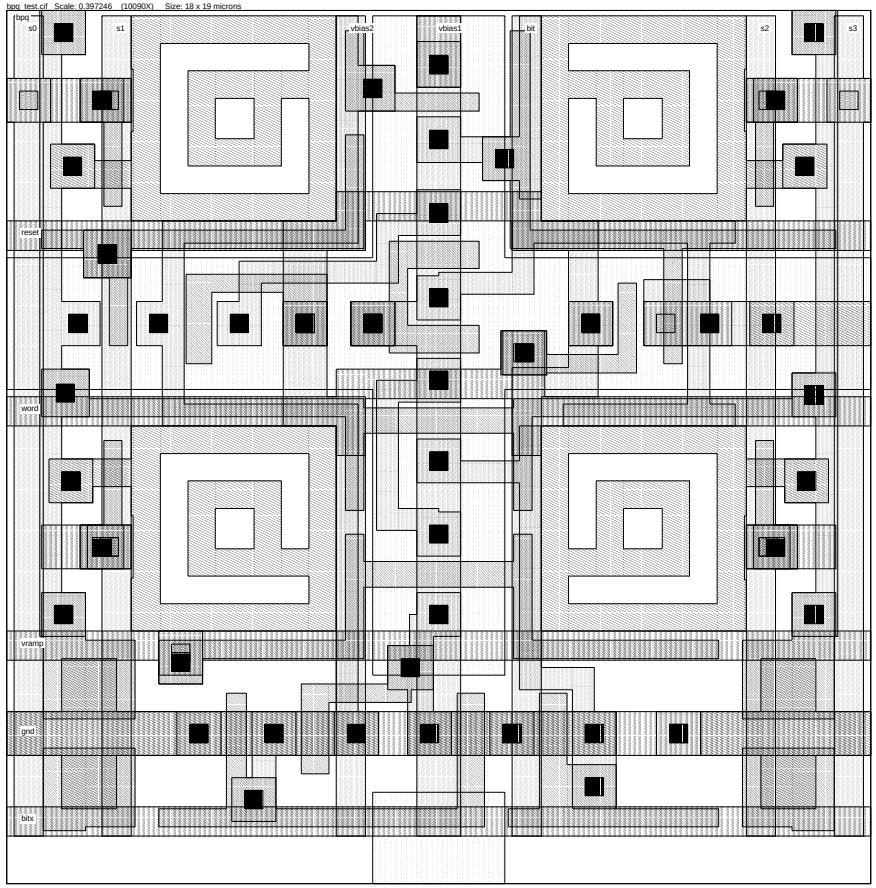
Output of Image Sensor with Pixel Level ADC



MCBS ADC Pixel Block Circuit Schematic - 18 Transistors



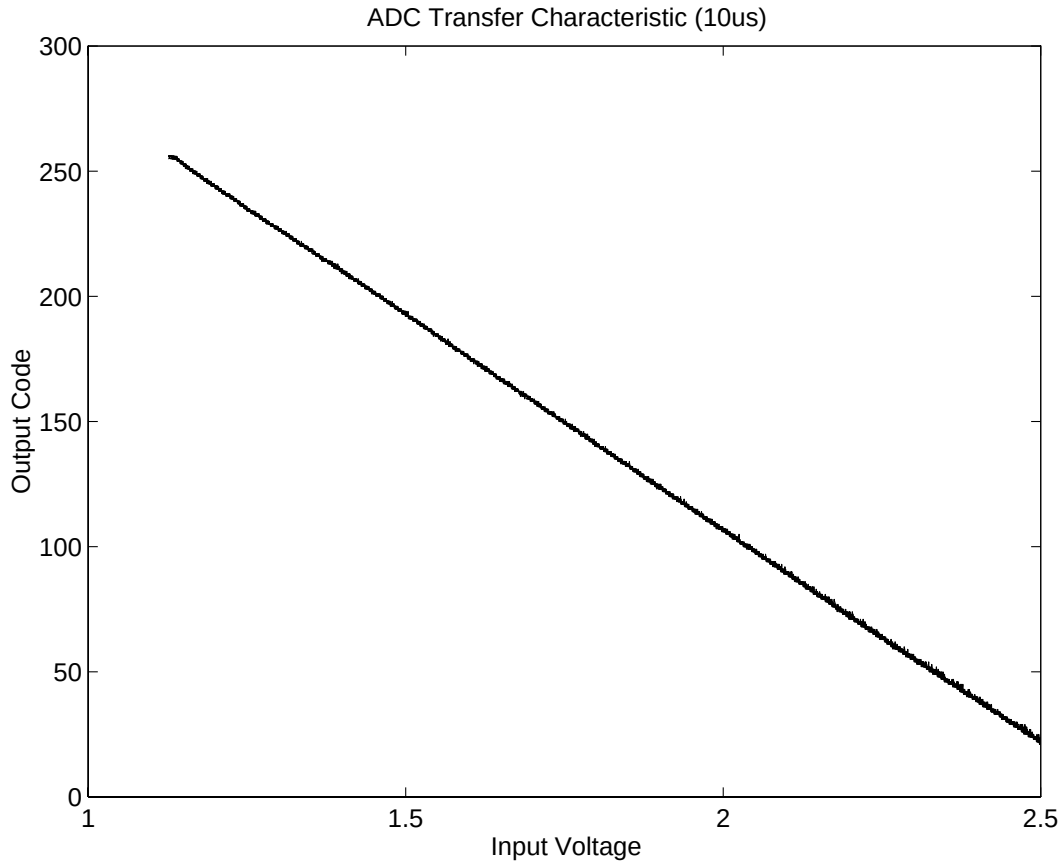
Nyquist Rate ADC Pixel Block Layout - 0.35μm, 8.9μm$\times$8.9μm



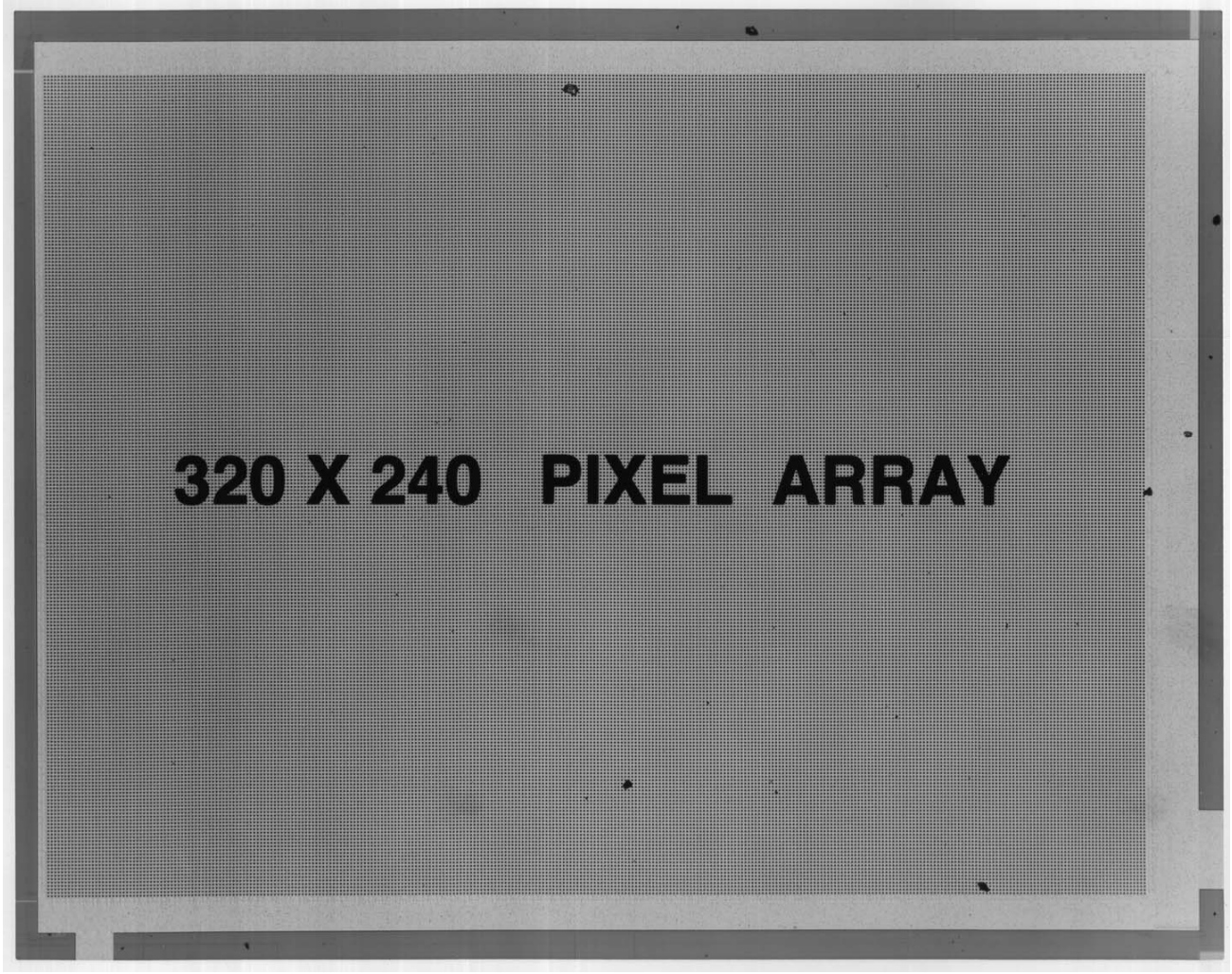
Main image sensor characteristics

Technology	0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS
Sensor Area	3027 μm $\times$ 2328 μm
Sensor size	320×240 pixels
Pixel Area	8.9 μm $\times$ 8.9 μm
Number of transistors per pixel	4.5 (18 per four pixels)
Fill Factor	25%
Package	224 pin PGA
Supply Voltage	3.3 V

Measured ADC Transfer Function



Die micrograph of 320×240 image sensor



Conclusion

- **First Nyquist rate pixel level ADC technique**
  - **Simple circuits**
  - **Very low power**
  - **Electrically testable**
- **A CMOS image sensor in a 0.35 μm 4 metal layer digital process**
  - **8.9$\times$8.9μm**
  - **25% fill factor**