

A 128×128 pixel CMOS Area Image Sensor with Multiplexed Pixel Level A/D Conversion

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Abstract

A 128×128 pixel CMOS area image sensor with a sigma-delta A/D Converter shared within each group of 2×2 pixels is described. Each pixel comprises a photodiode and 4 MOSFETs and occupies 20.8μm×19.8μm with a fill factor of 30% in a 0.8μm three layer metal one layer poly CMOS process. At 3.3V, the dynamic range is > 83dB, the dissipation is < 1mW and the fixed pattern noise is ≈1%.

Introduction

In digital imaging applications it is desirable to integrate A/D conversion with an area image sensor on the same chip. Such integration can significantly reduce power consumption and system cost. A number of approaches for integrating A/D conversion with image sensing have been developed [2, 3, 5, 4]. These approaches use CMOS technology because integration of sensing, A/D conversion and digital circuits on the same chip is difficult to accomplish with other image sensing technologies such as CCD. In [4] we proposed a pixel level A/D conversion approach using sigma-delta ($\Sigma\Delta$) modulation. The main advantage of such an approach is the use of very simple A/D conversion circuitry operating at low frequencies—in the kilohertz range—independent of the size of the sensor array. The low frequency also results in low power dissipation. An array of 64×64 pixels was fabricated in a 1.2μm two layer metal CMOS process. Each pixel consisted of a phototransistor and a first order $\Sigma\Delta$ A/D converter implemented using 22 MOS transistors. This approach had a large pixel size of 60μm×60μm and a low fill factor of 3%, relative to other image sensor approaches. In addition, the sensor suffered from unacceptably high fixed pattern noise of 10% due to beta variation of the phototransistors and MOS transistor mismatch in the $\Sigma\Delta$ A/D converters.

In this paper we describe an area image sensor that overcomes these limitations. The key idea is to share the $\Sigma\Delta$ A/D converter among four neighboring pixels through multiplexing. In addition more transistors are

saved by using an analog shift register for implementing the D/A converter. In the original design 8 MOS transistors were used for the D/A converter compared to only 3 for the new design. Finally, by using a photodiode instead of a phototransistor, fixed pattern noise is reduced. These improvements result in a reduction of the pixel size by a factor of 4, an increase in the fill factor to 30%, and a reduction of fixed pattern noise to 1%. Sharing circuit components in a pixel block not only reduces pixel size but also slightly increases the A/D converter uniformity. These improvements make our sensor approach comparable in density and image quality with other CMOS image sensors with integrated A/D conversion while achieving significantly lower power.

The remainder of this paper is organized as follows: first we describe the chip architecture of the 128×128 area image sensor. Then we discuss the pixel block design and implementation. Finally we present measurement results from our area image sensor.

Chip Architecture

Figure 1 shows a functional block diagram of the area image sensor. The chip consists of an array of 64×64 multiplexed pixel blocks, each consisting of a group of 4 nearest-neighbor pixels sharing a single A/D converter. Each pixel block is connected to a bit line using a pass transistor. The bit lines are “read” using a 6:64 row address decoder and an array of 64 digital sense amplifiers. The topology is identical to read only memory (ROM) circuits. Each pixel block converts the analog light intensity into a digital code. The entire system is synchronous and after each clock pulse every pixel block produces one bit of data. This generates a two dimensional array of bits or a “bit plane”. One frame of video data consists of L bit planes.

Since we have selected to use pixel-level A/D conversion, each A/D converter must be constructed using a very small amount of silicon area. The A/D converter’s size is inversely proportional to the number of pixels in the sensor, and to the fill factor of each pixel. Con-

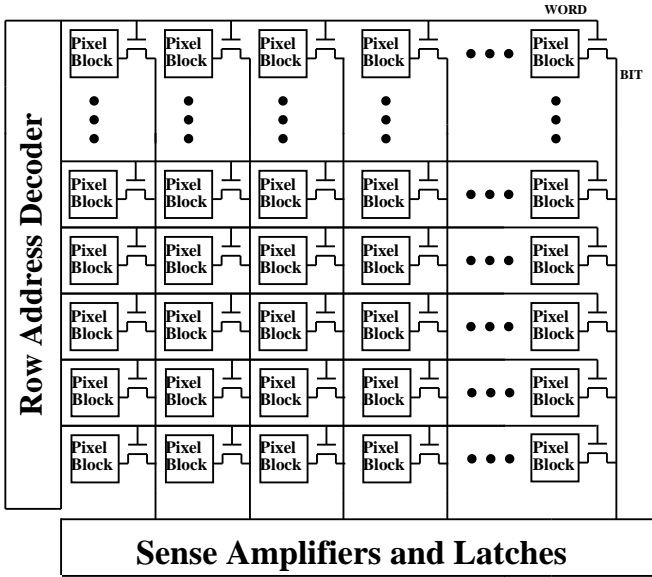


Figure 1: Image Sensor Chip Functional Block Diagram

ventional Nyquist A/D conversion techniques require too much silicon area. We found that oversampled A/D conversion methods provide a reasonable compromise between size and functionality. Specifically, we chose first order one-bit $\Sigma\Delta$ A/D conversion because it is simple, and robust to process variation and system noise.

Figure 2 shows a first order one-bit $\Sigma\Delta$ A/D converter [1]. It consists of an integrator and a one bit quantizer.

The $\Sigma\Delta$ A/D converter generates data at L times the Nyquist rate. The oversampled data is decimated to the Nyquist rate using a digital low pass filter. The resulting SNR of the Nyquist rate data can be computed as

$$\text{SNR} = 9 \log_2 L - 5.2 \text{dB}.$$

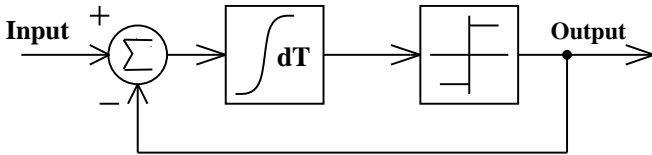


Figure 2: $\Sigma\Delta$ A/D converter.

Pixel Design

A circuit schematic of the multiplexed pixel block is given in Figure 3. Each photodiode in the multiplexed pixel block is formed by using an n+ diffusion in a p substrate. The photodiodes are reverse biased and exposed to light, while the rest of the circuitry is covered with the third

layer of metal to reduce the chance of photon induced latch-up.

The multiplexed pixel block operates as follows. The pixels are selected one at a time using the select signals **S0**, **S1**, **S2**, and **S3**. (Figure 4 shows the control signal waveforms when pixel D0 is selected.) $\Sigma\Delta$ A/D conversion is performed on the photocurrent generated by each pixel. This current is integrated by the photodiode junction capacitance. The junction voltage of the selected photodiode is quantized using a comparator with regenerative feedback clocked via **CK**. The comparator is biased subthreshold in order to reduce power and noise, increase gain, and reduce any leakage current in the D/A converter. The quantized value is converted to a current using a 1 bit D/A converter and feedback to the photodiode. The 1-bit D/A is implemented by an analog shift register similar to a 3-phase CCD transfer structure. After a sequence of 3 control pulses **DUMP**, **STORE**, **CK** (as shown in Figure 4), a fixed amount of charge is dumped on the junction capacitance if the output of comparator **FEEDBACK** is low. The voltage of **STORE** can be used to control the amount of charge transferred to the junction capacitance. Therefore, electronic shuttering can be performed by adjusting **STORE**'s voltage. At the completion of each clock cycle a single bit is generated and read out using the bit line **BIT**.

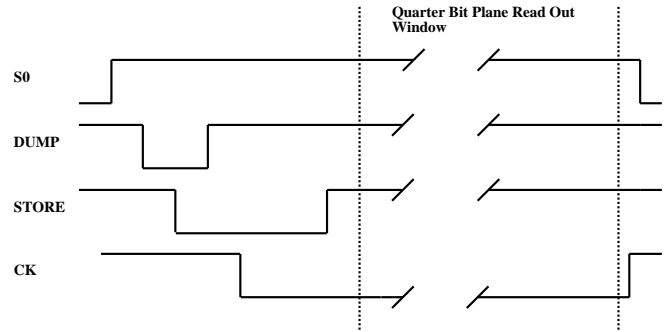


Figure 4: Control Signal Waveforms.

The area image sensor chip operates as follows: after an image is focused on the chip, the $\Sigma\Delta$ A/D converters are globally clocked at a rate F_s well above the Nyquist image frame rate, $2F_d$. First the top left pixel (D0) in each pixel block is selected by asserting **S0**. At the end of the clock cycle the outputs of the $\Sigma\Delta$ converters form a 64×64 array of bits, referred to as a “quarter bit plane”, which is read out one row at a time. The quarter bit planes corresponding to D1, D2, and D3 are then read out in the same manner. The four quarter bit planes form a single “bit plane” of the image. The image is fully captured using a number of bit planes determined by the target SNR [4]. SNR degradation due to charge injection

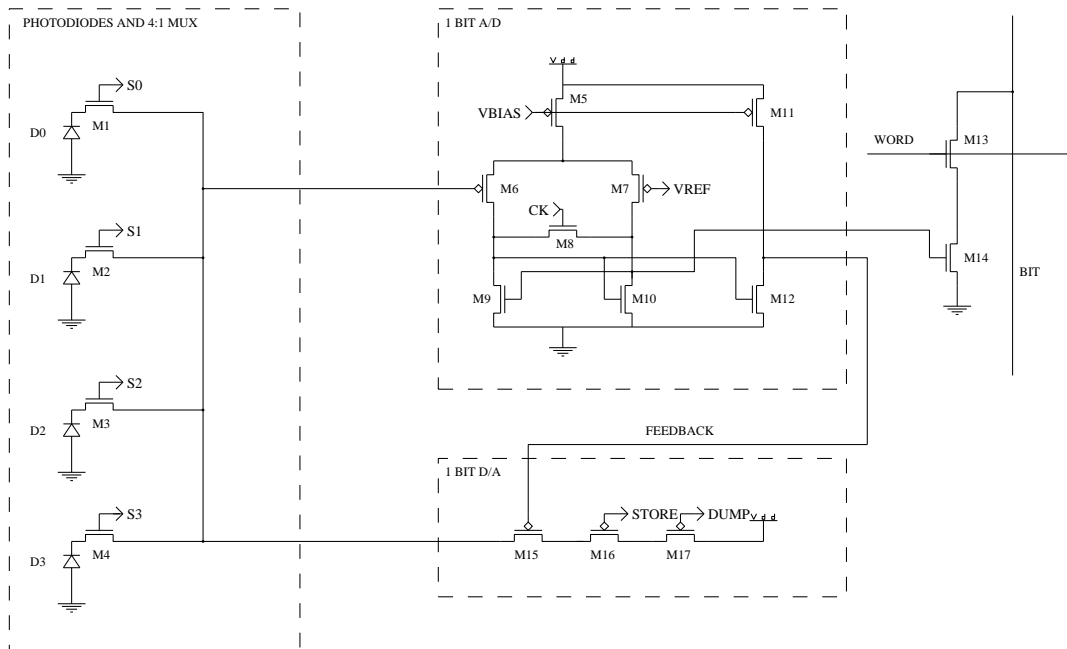


Figure 3: Circuit Schematic of Multiplexed Pixel Block.

of the digital circuitry in close proximity to the analog sensors is negligible since the frequency of operation—kilohertz range—is very low.

Measured Results

To characterize the new area image sensor we designed and fabricated a 128×128 pixel sensor using a $0.8 \mu\text{m}$ three layer metal single layer poly CMOS technology. Figure 7 shows the die photo. The chip is functional and Figure 5 shows the measured output from a single pixel's $\Sigma\Delta$ converter as a function of time. To reconstruct the digitized pixel value a decimation filter [1] is used. This can be implemented in software or with the addition of on chip digital FIR filters and an external memory. For example, the lower graph in Figure 5 shows 3 'ones' in 8 clock cycles; if we use a counter as a simple decimation filter, the pixel output is $3/8$ of the maximum output value.

Figure 6 is obtained by the sensor in room light. The images are focused onto the chip using an 8-mm lens.

In the process of switching between the multiplexed pixels, charge sharing occurs. This effect has been simulated and results show that charge sharing does not smear the image, on the contrary it performs slight edge enhancement.

The sensor achieves a dynamic range¹ greater than 83dB. This is the case since the magnitude of the feedback D/A converter can be varied by a factor of 40dB, and the maximum measured SNR at a frame rate of 30Hz and an oversampling ratio of 64 is approximately 43dB.

¹The ratio of the maximum non-saturating photocurrent to the dark current.

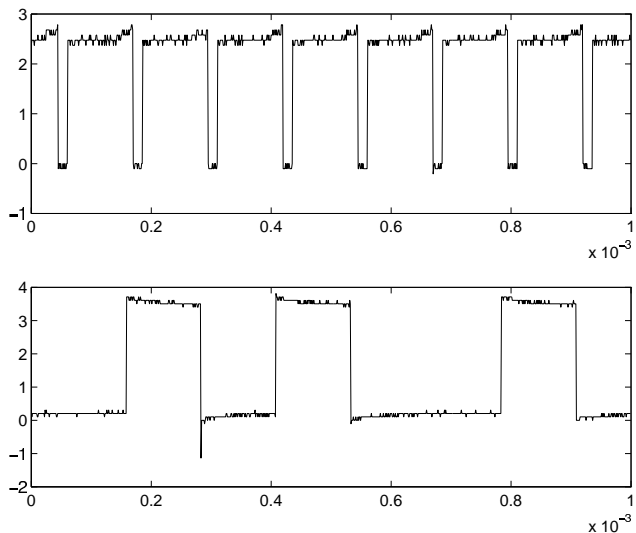


Figure 5: Single pixel $\Sigma\Delta$ A/D converter output from HP54601A. The top graph is **CK** bar and the bottom graph is the pixel output verses time.



Figure 6: Image Obtained by the Sensor.

The fixed pattern noise was calculated to be approximately 1% using measured results from the D/A converter and photodiode.

The sensor, without pads, consumes less than 1 mW. The static current of each pixel is approximately 1nA, and the dynamic current for the entire array is less than 200 μ A. We summarize the main characteristics of the chip in Table 1.

Table 1: Area Image Sensor Characteristics
128x128 Area Image Sensor Characteristics

Technology	0.8 μ m, 3-layer metal, 1-layer poly, nwell CMOS
Die Area	3337 μ m \times 3200 μ m
Pixel Area	20.8 μ m \times 19.8 μ m
Transistors per pixel	4.25 (17 per four pixels)
Fill Factor	30%
Package	65 pin PGA
Supply Voltage	3.3v
Dynamic Range	83dB
Dissipation w/o Pads	< 1 mW
Fixed Pattern Noise	\approx 1%
Measurement Temperature	21 $^{\circ}$ C

Conclusion

We have demonstrated a CMOS area image sensor with multiplexed pixel level A/D conversion. This multiplexed pixel design substantially improves the work reported in [4]. With a fill factor of 30% and a pixel size of 20.8 μ m \times 19.8 μ m, our sensor is comparable in density and image quality with other CMOS image sensors with integrated A/D conversion while achieving significantly lower

power. Additionally, our sensor topology scales well with CMOS technology advances. For example, the speed of each A/D converter is independent of the sensors size.

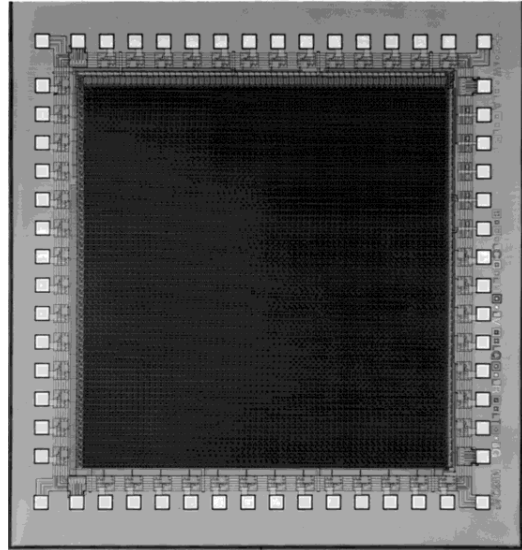


Figure 7: 128 \times 128 Image Sensor Chip Micrograph.

Acknowledgments

We thank M. Godfrey for his contribution to the test bed, and H. Elabd for his contribution to our new D/A converter circuit. We also thank B. Wooley and M. Horowitz for their support and encouragement, DARPA for funding fabrication through MOSIS, and Hewlett Packard, Intel, AMD, Interval Research and MSIS for their support of the Information Systems VLSI lab.

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