ANALYSIS OF APS READOUT CIRCUIT DELAY

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ABSTRACT

The paper provides a complete analysis of the APS pixel and column circuit delay. Contrary to common belief, we show that shorter settling times can be achieved by reducing the bias current and hence reducing energy consumption. We then investigate the effect of non-idealities on the readout operation. We find that when the follower transistor channel length modulation is taken into consideration, delay is reduced, which implies that shorter length transistors can be used in the pixel. As expected, we find that delay decreases linearly with technology scaling.

1. INTRODUCTION

An important advantage of CMOS APS is its high frame rate capability [1]. In [2] Krymski *et al.* describe a 1024×1024 APS with column level ADC achieving frame rate of 500 frames/s. In [3] Stevanovic *et al.* describe a 256×256 APS with 64 analog outputs achieving frame rate of 1000 frames/s. Recently high speed CMOS APS based digital cameras have become commercially available [4]. The high frame rate capability of CMOS APS combined with the a-bility to integrate processing on the same chip can also be used to enable new applications and to improve the performance of existing applications as discussed in [5, 6].

Although the operation of CMOS APS is quite standard and has been extensively reported on, to the best of our knowledge no complete analysis of its readout circuit delay has been reported, especially for deep sub-micron technologies. A better understanding of the readout circuit would help in optimizing its frame rate.

In this paper we provide a complete analysis of the s-tandard APS pixel and column readout circuit delay. Our analysis includes such non-idealities as the access transistor resistance, channel length modulation, and non-square law saturation current. The analysis is first performed assuming a standard 0.35μm CMOS technology. Contrary to common belief, we find that shorter settling times can be achieved by reducing the bias current and hence reducing energy consumption. We find that when the follower transistor channel length modulation is taken into consideration,

delay is reduced, which implies that shorter length transistors can be used resulting in a higher fill factor. The analysis is then extended down to 0.1μm. As expected, we find that delay improves linearly with technology scaling.

The rest of the paper is organized as follows. In the following section we analyze the APS readout circuit delay assuming a 0.35μm CMOS technology. In Section 3 we analyze the effect of the non-idealities on circuit delay. In the last section we discuss the effect of technology scaling on readout delay.

2. APS CIRCUIT OPERATION

The basic APS circuit is shown in Figure 1. After photocurrent integration the access transistor is activated by applying a high signal on its gate. Ideally the access resistance should be zero, leading to $v_o = v_{of}$. Considering level one model for both the bias and follower transistors, (*i.e.*, no channel length modulation), KCL at the output node gives

$$I_b + C_T \frac{dv_o}{dt} = K_n(v_{in} - v_{TF} - v_o)^2.$$

This differential equation can be readily solved analytically by separation of variables and the output voltage, $v_o(t)$, is given by

$$v_o(t) = v_{in} - v_{TF} - \rho\left(\frac{1 + \frac{\alpha-\rho}{\alpha+\rho}e^{\frac{-2\rho K_n}{C_T}t}}{1 - \frac{\alpha-\rho}{\alpha+\rho}e^{\frac{-2\rho K_n}{C_T}t}}\right),$$

where $\rho = \sqrt{\frac{I_b}{K_n}}$, and $\alpha = v_{in} - v_{TF} - v_o(0)$.

In most APS implementations aimed at high frame rate operation, each column, or group of columns, share an ADC (*e.g.*, [2]). The *settling time* T_s is defined as time from the access transistor turning on to the output voltage v_o reaching to within half a bit of its steady state value. For worst case delay, we set the input voltage v_{in} to its maximum possible value and assume that the output voltage before switching is at its lowest possible value, $v_o(0)$. Under these conditions, the settling time is given by

$$T_s = \frac{C_T}{2\sqrt{K_n * I_b}} \ln\left(\frac{(\beta + \rho)(\alpha - \rho)}{(\beta - \rho)(\alpha + \rho)}\right), \text{ where}$$
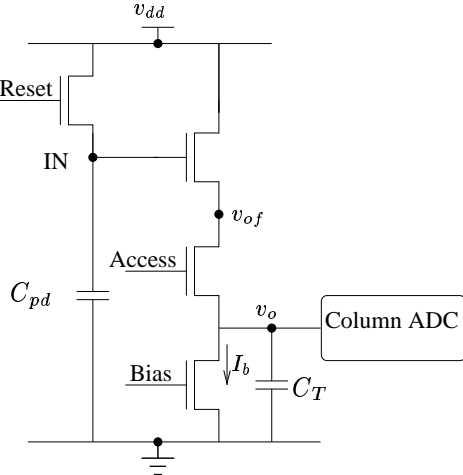
Fig. 1. APS circuit schematic.

$$\beta = v_{in} - v_{TF} - v_o(T_s),$$

$$v_o(T_s) = (1 - \frac{1}{2^{n+1}})(v_o(\infty) - v_o(0)) + v_o(0), \text{ and}$$

$$v_o(\infty) = v_{in} - v_{TF} - \sqrt{\frac{I_b}{K_n}}.$$

Figure 2 plots settling time, T_s, versus bias current I_b assuming typical $0.35\mu m$ technology parameters. Note that decreasing bias current leads to shorter settling time, since more current is available to charge the output node.
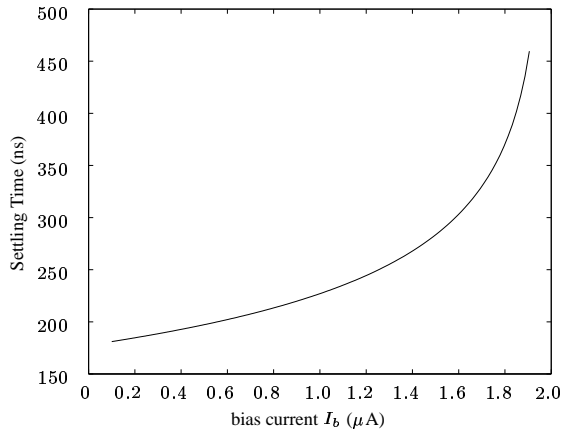

Fig. 2. APS settling time variation with bias current.

Reducing bias current also leads to an increase in output voltage swing, S, which is given by

$$S = v_o(\infty) - v_o(0) = v_{in} - v_{TF} - \sqrt{\frac{I_b}{K_n}} - v_o(0).$$

The voltage swing versus the bias current is plotted in Figure 3.

The energy consumed by the APS circuit during readout can be calculated by integrating the power consumed during readout, which gives

$$E = C_T Vdd(\frac{\rho}{2} \ln{(\frac{(\beta + \rho)(\alpha - \rho)}{(\beta - \rho)(\alpha + \rho)})} + v_o(0) - v_o(T_s)).$$

As bias current is reduced from $1.9\mu A$ to $0.1\mu A$ the energy consumed drops by 20% as shown in Figure 4, while settling time is reduced by as much as 50% as shown in Figure 2. Thus, contrary to common belief, delay can be reduced while consuming less energy.
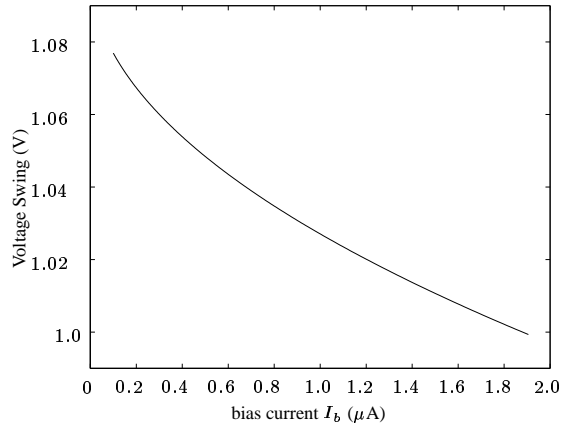

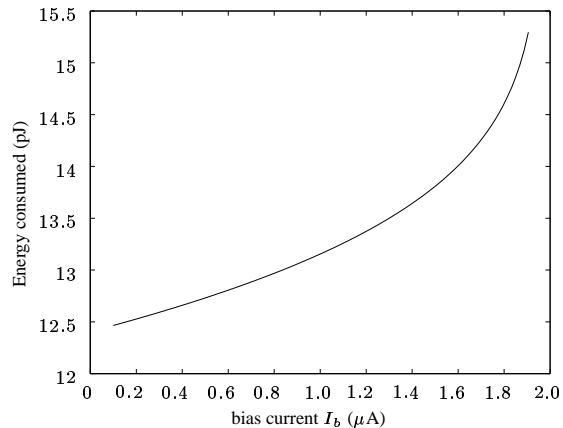**Fig. 3**. Output swing versus bias current.

Fig. 4. APS energy consumed variation with bias current.

3. EFFECT OF NON-IDEALITIES

In this section we investigate the effect of circuit non-idealities, namely, non-zero access transistor resistance, R_a, current source channel length modulation λ_i, and follower transistor channel length modulation λ_f. With these non-idealities

included, the circuit equations are

$$I_f = \frac{v_{of} - v_o}{R_a},$$

$$I_f = I_b(1 + \lambda_i v_o) + C_T \frac{dv_o}{dt}, \text{ and}$$

$$I_f = K_n(v_{in} - v_{TF} - v_{of})^2(1 + \lambda_f(v_{dd} - v_o)).$$

To investigate the effect of each non-ideality separately, we set the terms corresponding to the other two to zero and solve the set of equations. First we consider the effect of the non-zero access transistor resistance, R_a, on settling time, and get that

$$T_s = \frac{C_T}{2\sqrt{K_n * I_b}} \ln\left(\frac{(\beta + \rho)(\alpha - \rho)}{(\beta - \rho)(\alpha + \rho)}\right) + R_a C_T \ln\left(\frac{\alpha^2 - \rho^2}{\beta^2 - \rho^2}\right).$$

Note that decreasing the access transistor resistance, which can be done by increasing its width, reduces settling time. This, however, is not desirable, since it leads to larger pixel size or smaller fill-factor. Fortunately, this effect can be mitigated using lower bias current as shown in Figure 5.
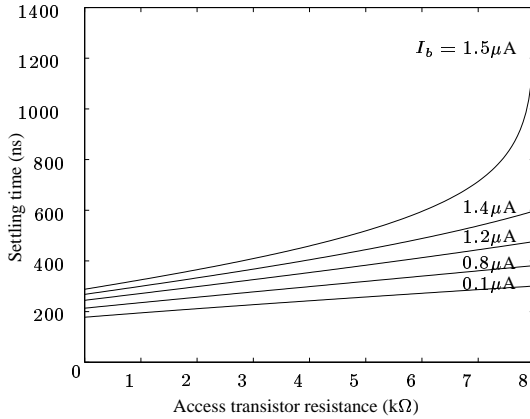

Fig. 5. APS settling time variation with access resistance for different I_b.

Now we consider the current source transistor channel length modulation. We set R_a and λ_f to zero. In this case the settling time is given by

$$T_s = \frac{C_T}{2K_n\rho} \ln\left(\frac{(\beta + \rho)(\alpha - \rho)}{(\beta - \rho)(\alpha + \rho)}\right),$$

where

$$\beta = \frac{\lambda_i I_b}{2K_n} + v_{in} - v_{TF} - v_{omax},$$

$$\alpha = \frac{\lambda_i I_b}{2K_n} + v_{in} - v_{TF} - v_{omin}, \text{ and}$$

$$\rho = \sqrt{\frac{I_b(1 + \lambda_i(v_{in} - v_{tf}))}{K_n} - \left(\frac{\lambda_i I_b}{2K_n}\right)^2}.$$

This is plotted in Figure 6. Note that settling time increases when the effect of the channel length is taken into consideration, due to the reduction in the current available to charge the output node. Since the channel length modulation is inversely proportional to the the transistor gate length, λ can be decreased by increasing the transistor channel length. Therefore, increasing the current source transistor gate length reduces settling time. This can be done with no effect on pixel size or fill-factor, since the current source is part of the column level circuits.
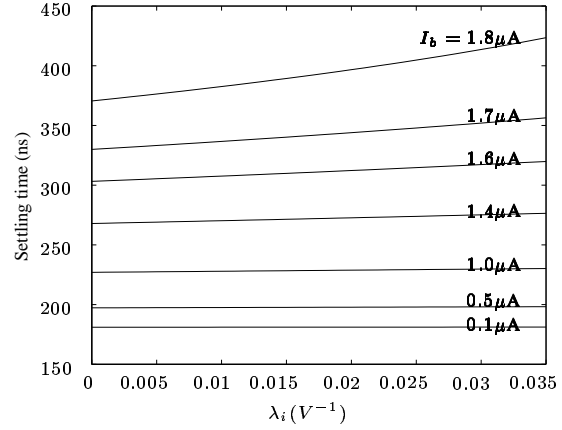

Fig. 6. APS settling time versus lambda of the current source.

Finally we consider the effect of the follower transistor channel length modulation. The result is plotted in Figure 7. As shown in the figure, settling time decreases as λ_f increases, due to the increase in the current available to charge the output node (for a given bias current). Therefore, settling time can be decreased by making the follower transistor channel length as small as possible. Other considerations, such as off current, may preclude the use of a minimum channel length transistor, however.

Figures 6 and 7 also show that reducing bias current not only reduces settling time, but also diminishes the effect of channel length modulation.

4. TECHNOLOGY SCALING

As technology scales the square law drain saturation current relation becomes less accurate. A more accurate model for the follower current is given by

$$I_f = K_n(v_{in} - v_{TF} - v_o)^\gamma, \text{ for } 1 < \gamma < 2.$$

In this case, neglecting non-idealities, the settling time can be readily calculated to be

$$T_s = \frac{C_T}{K_n} \sum_{j=1}^{\infty} \left(\frac{I_b}{K_n}\right)^{j-1} \frac{1}{(j\gamma - 1)}\left(\frac{1}{\beta^{(j\gamma-1)}} - \frac{1}{\alpha^{(j\gamma-1)}}\right).$$
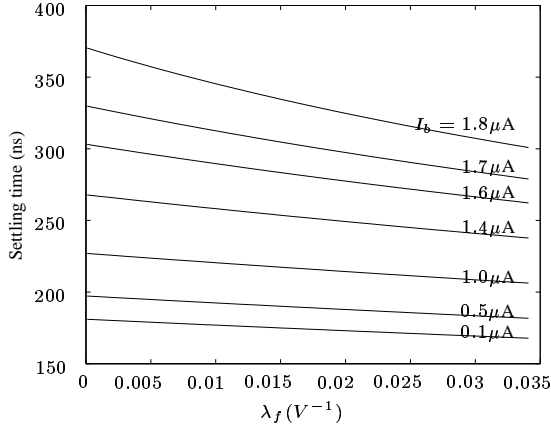
Fig. 7. APS settling time versus lambda for the follower transistor.

This is plotted in Figure 8. As technology scales, settling time decreases and the effect of the bias current becomes less pronounced.
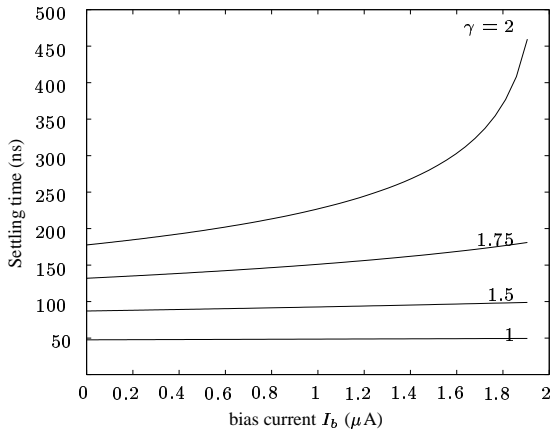

Fig. 8. APS settling time versus bias current for different γ.

Figure 9 plots the settling time for technologies down to 0.1μm. The device and circuit parameters used in the simulations are from [7]. Note that settling time decreases almost linearly with minimum feature size.

5. CONCLUSION

We presented a complete analysis of the APS pixel and column circuit delay. Contrary to common belief, we showed that shorter settling times can be achieved by reducing the bias current and hence reducing energy consumption. We then investigated the effect of non-idealities on the readout operation and found that when the follower transistor channel length modulation is taken into consideration, delay is reduced. As expected, we found that delay improves linear-
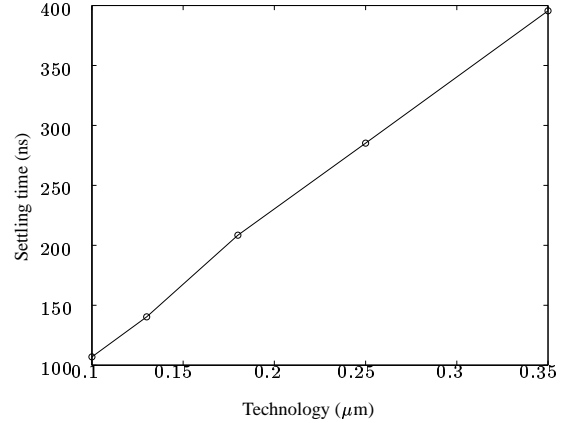

Fig. 9. Settling time versus minimum feature size.

ly with technology scaling.

6. ACKNOWLEDGEMENTS

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