

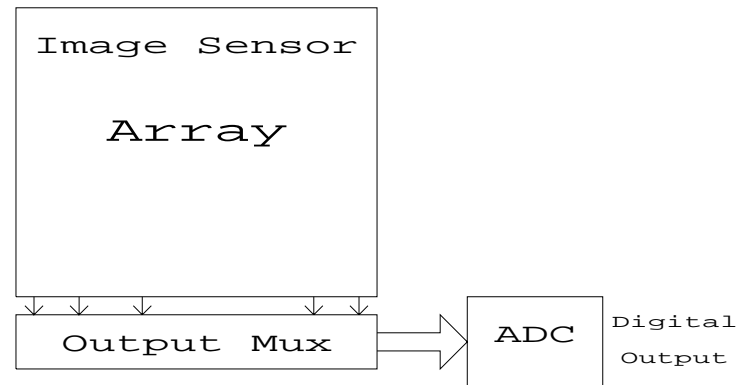
Techniques for Pixel Level Analog to Digital Conversion

Boyd Fowler, David Yang, and Abbas El Gamal

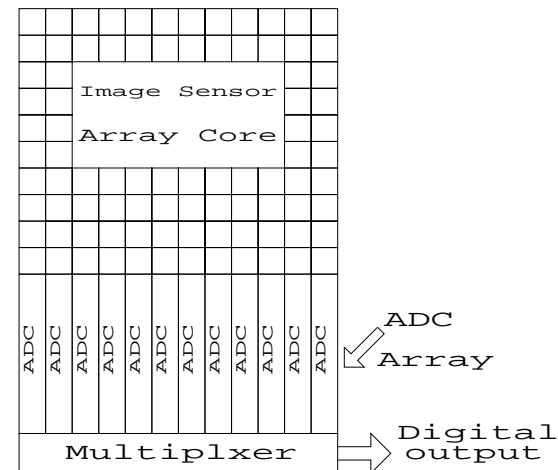
Stanford University

Approaches to Integrating ADC with Image Sensor

- Chip Level



- Column Level



- Pixel Level

Pixel Level ADC

- Advantages

- Continuous observation of the pixel
- Low noise
- Low power

- Disadvantages

- Limited area at the pixel level – this becomes less of a problem as technology scales

Outline

- ⇒ • **Architecture**
 - $\Sigma\Delta$ ADC
 - MCBS ADC
 - Readout circuitry

- **Circuits**
 - $\Sigma\Delta$ pixel
 - MCBS pixel

- **Results**

- **Comparision**

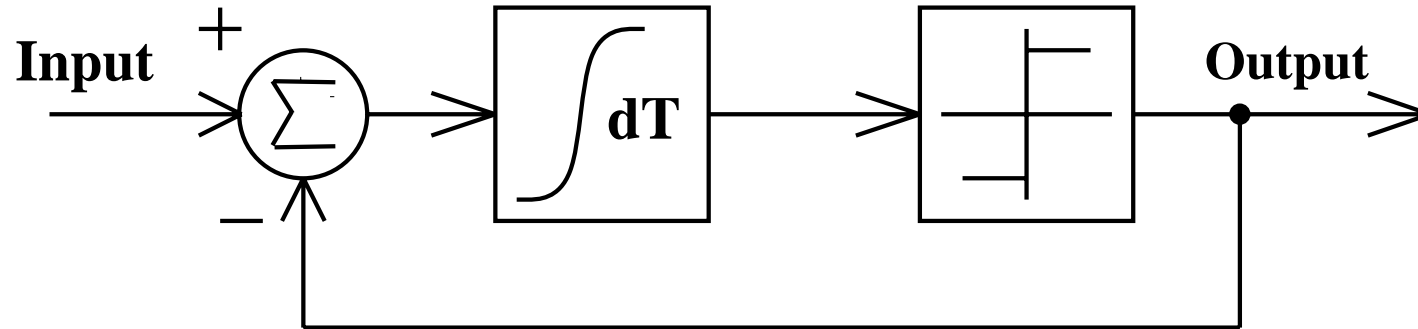
Pixel Level ADC

- Pixel size limits ADC architecture
- Cannot use conventional bit-parallel ADC techniques, because they require memory at the pixel
- Bit serial ADC is required but conventional techniques are too complicated
- To overcome this problem we developed two bit serial techniques
 - Oversampled
 - Nyquist rate

Oversampled ADC

- Robust operation over process variation and noise
- Simple imprecise circuits can be used
- Use first order 1 bit $\Sigma\Delta$ modulation
 - Requires small silicon area

First Order 1 Bit $\Sigma\Delta$ Modulation



Output decimated using LPF to obtain pixel values - performed off chip.

Oversampling Ratio L as a function of SNR

Number of bit planes L per frame for a desired average SNR

$$\log_2(\mathbf{L}) = \frac{\mathbf{SNR} + 5.2\text{dB}}{9.0}$$

Examples:

- SNR = 48dB (8 bits) \Rightarrow L = 60
- SNR = 20dB (3.3 bits) \Rightarrow L = 7

$\Sigma\Delta$ ADC Limitations

- Increased output bandwidth caused by oversampling
- Decimation/DSP is required to resample the data at the Nyquist frequency
- Poor low light response due to nonuniform quantization

Pixel Level Nyquist Rate ADC

Recently developed a new multi-channel bit-serial (MCBS) ADC technique (Yang, Fowler, El Gamal CICC'98)

- Low output data rate
- Requires very few transistors at the pixel
- Uses very simple circuits
- Complex circuits shared by all pixels
- No external DSP is required to construct image

MCBS ADC

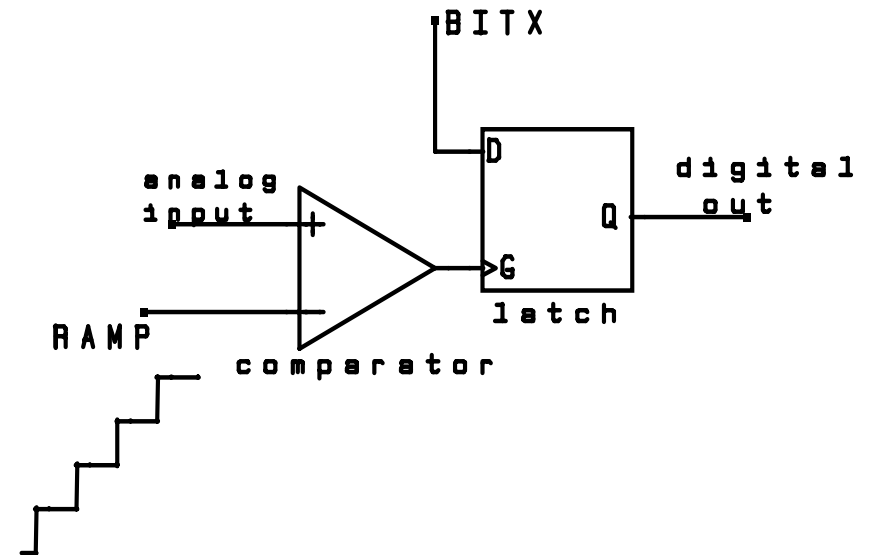
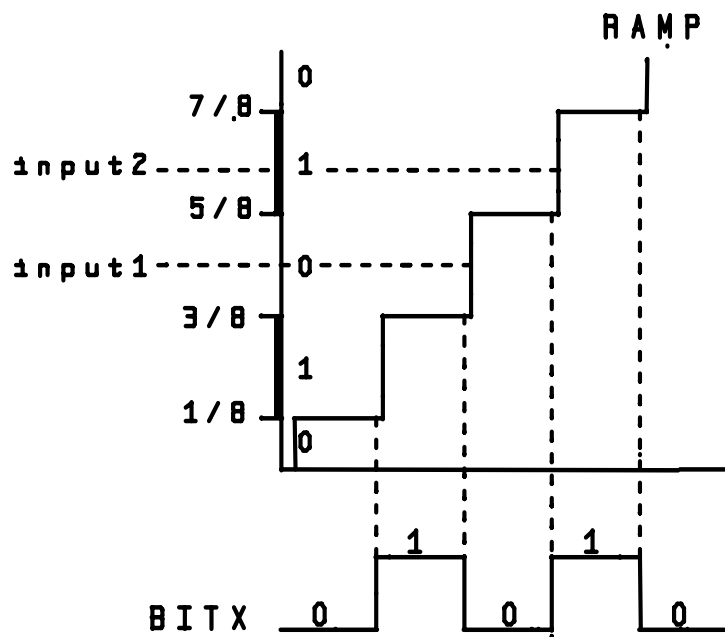
ADC assigns binary codewords to quantization intervals
3-bit example: signal $S \in [0, 1)$

Quantization table	
S	Gray Code
$0 - \frac{1}{8}$	0 0 0
$\frac{1}{8} - \frac{2}{8}$	0 0 1
$\frac{2}{8} - \frac{3}{8}$	0 1 1
$\frac{3}{8} - \frac{4}{8}$	0 1 0
$\frac{4}{8} - \frac{5}{8}$	1 1 0
$\frac{5}{8} - \frac{6}{8}$	1 1 1
$\frac{6}{8} - \frac{7}{8}$	1 0 1
$\frac{7}{8} - 1$	1 0 0

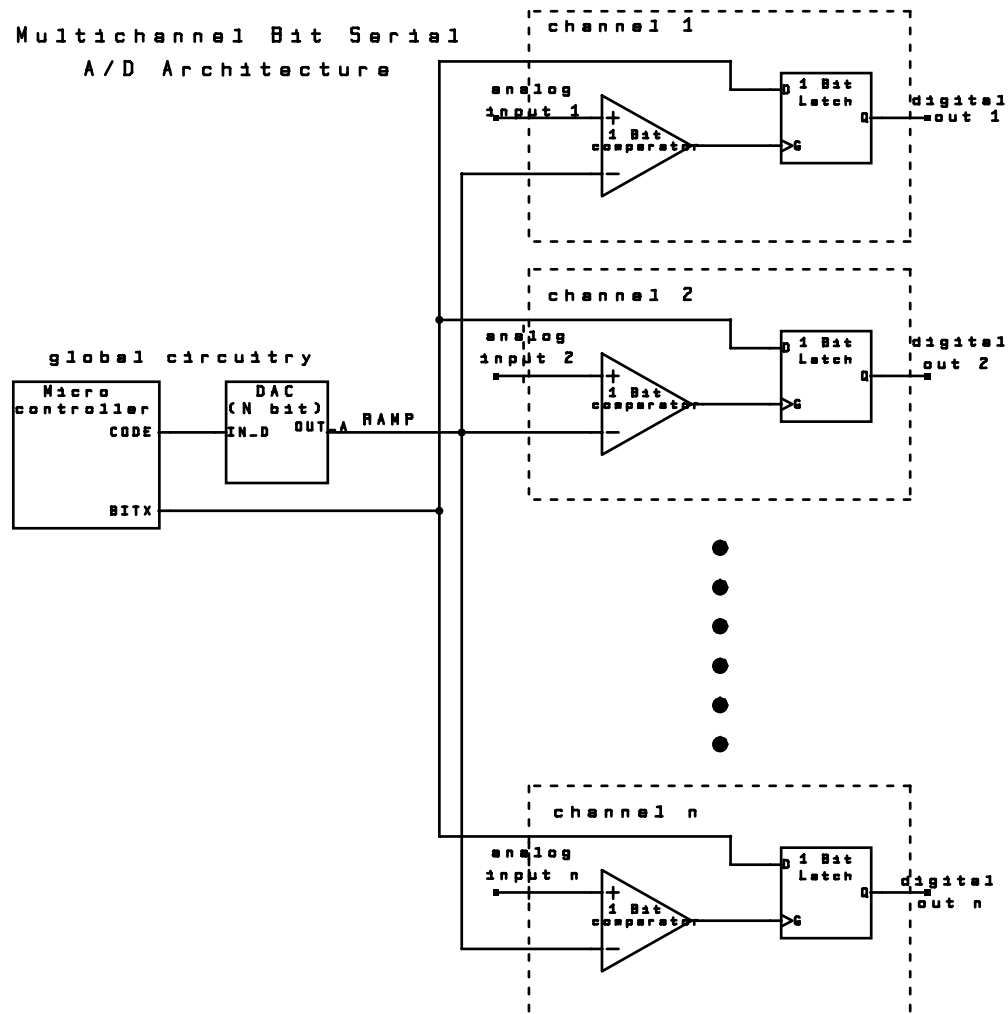
Key observation: Each output bit can be viewed as a binary-valued function over intervals (independent of other bits!)

Operation of the 1-bit Comparator/Latch

3 Bit LSB Example



MCBS ADC – Block Diagram

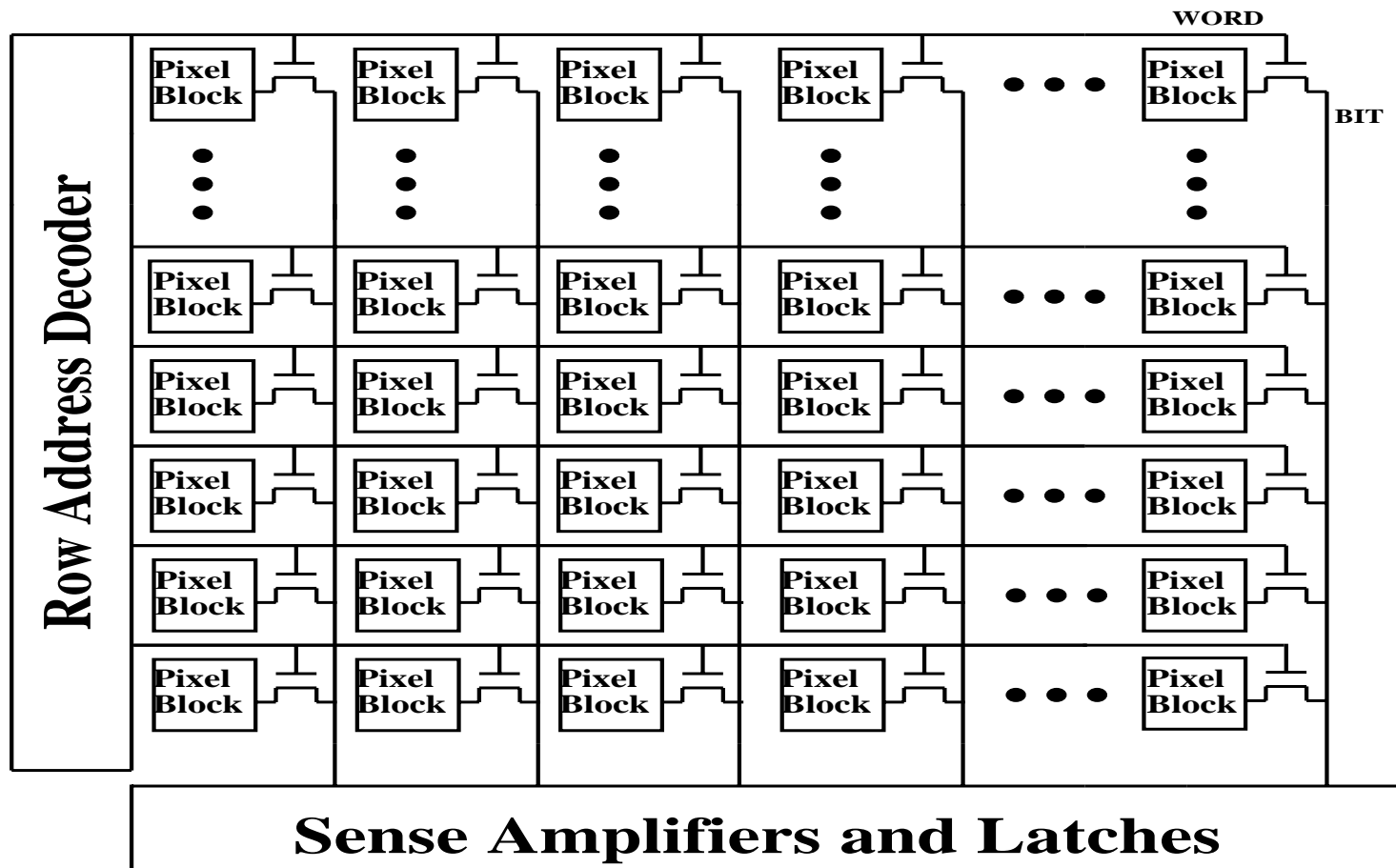


MCBS ADC Limitation

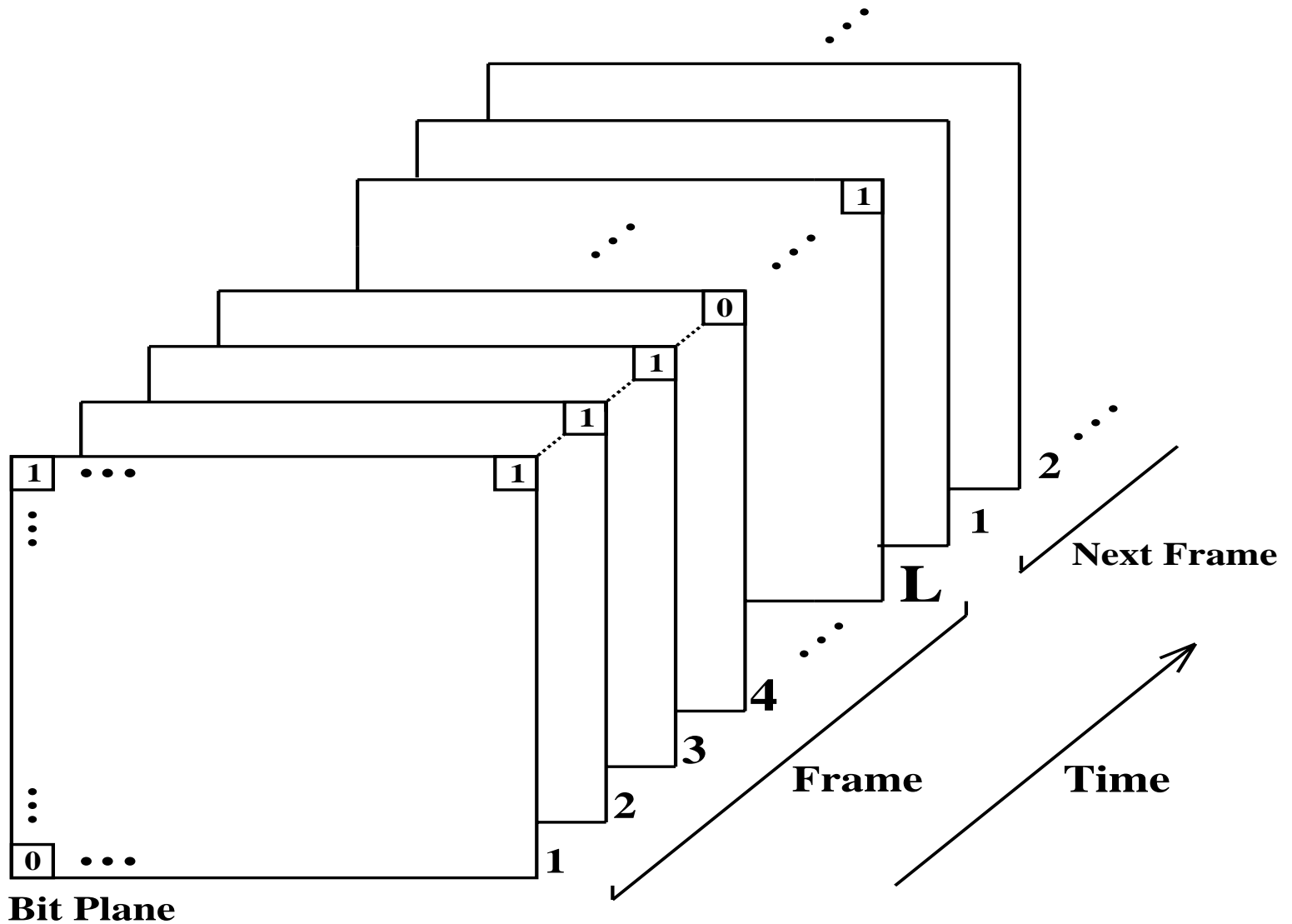
The gain bandwidth product must exceed $2F_d \times 4^m$

- To perform m bit quantization at least $2^m - 1$ comparison must be performed
- Assuming uniform quantization, the gain of the comparator must be proportional to 2^m .

Block Diagram for Image Sensor with Pixel Level ADC



Output of Image Sensor with Pixel Level ADC



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Multiplexed $\Sigma\Delta$ Pixel Block Diagram - 17 Transistors

Multiplexed $\Sigma\Delta$ Pixel Block Circuit Schematic - 17 Transistors

$\Sigma\Delta$ ADC Circuit

- Advantages

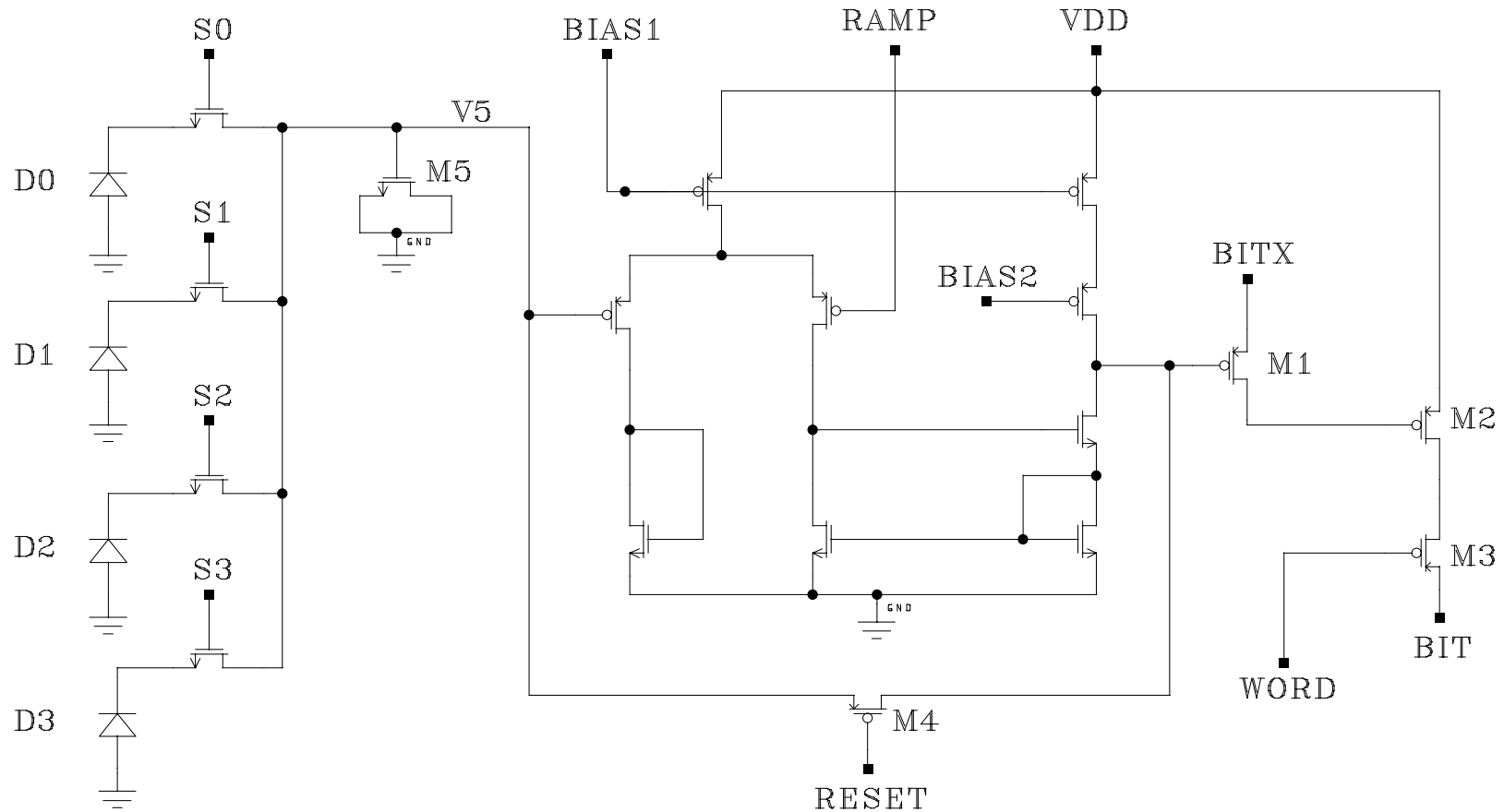
- Small size
- Low sensitivity to transistor noise, and no offset FPN
- Large charge handling capacity

- Disadvantages

- Moderate gain FPN
- Poor low light response
- High output data rate

MCBS ADC Pixel Block Circuit Schematic - 19

Transistors



MCBS ADC

- Advantages

- Small size
- Low gain and offset FPN
- Complete testability

- Disadvantages

- Moderate comparator gain-bandwidth
- Reduced sensitivity caused by sample capacitor

Outline

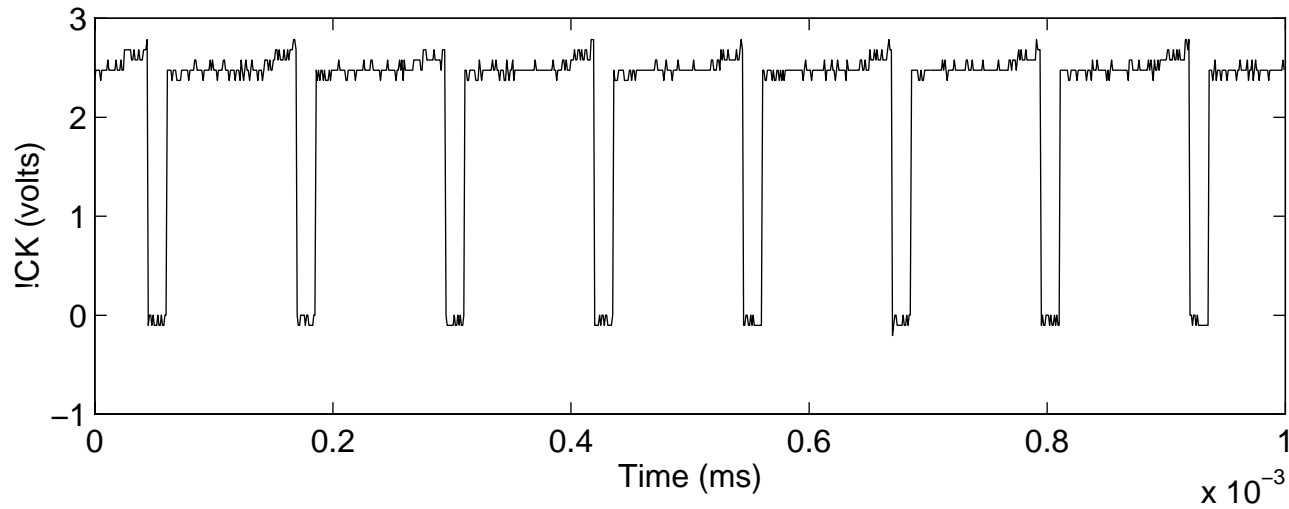
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Chip Characteristics

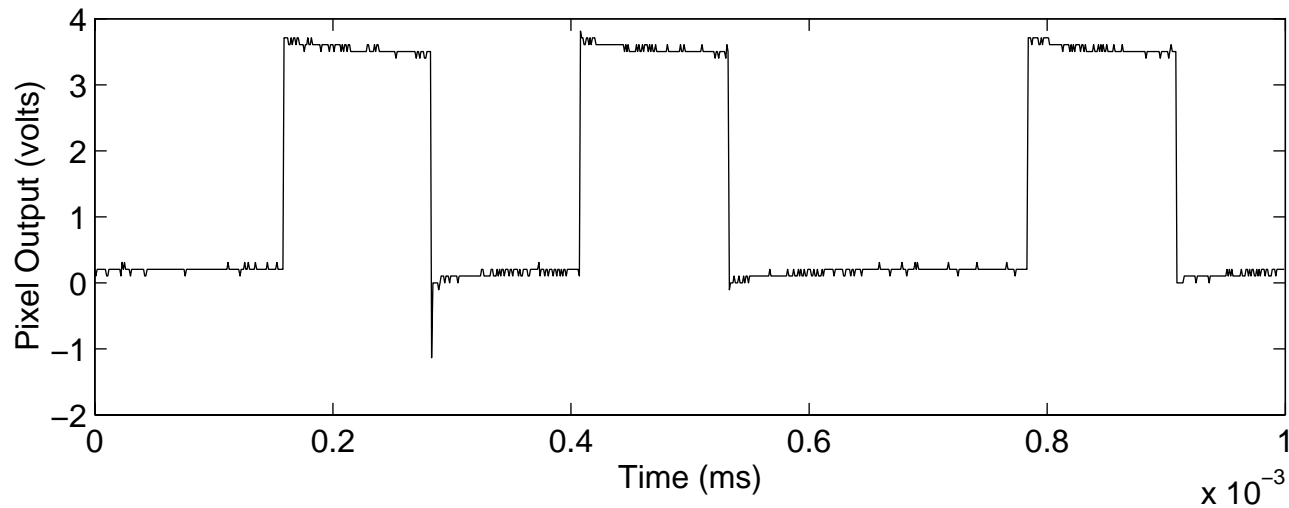
	$\Sigma\Delta$ ADC	MCBS ADC
Technology	0.8 μm 3M1P	0.35 μm 4M1P
Pixel Area	20.8 μm \times 19.8 μm	8.9 μm \times 8.9 μm
Transistors per pixel	4.25 (17 per four pixels)	4.5 (18 per four pixels)
Fill Factor	30%	25%
Array Size	128 \times 128	320 \times 240
Supply Voltage	3.3 v	3.3 v

$\Sigma\Delta$ ADC Output Waveforms

CLKB

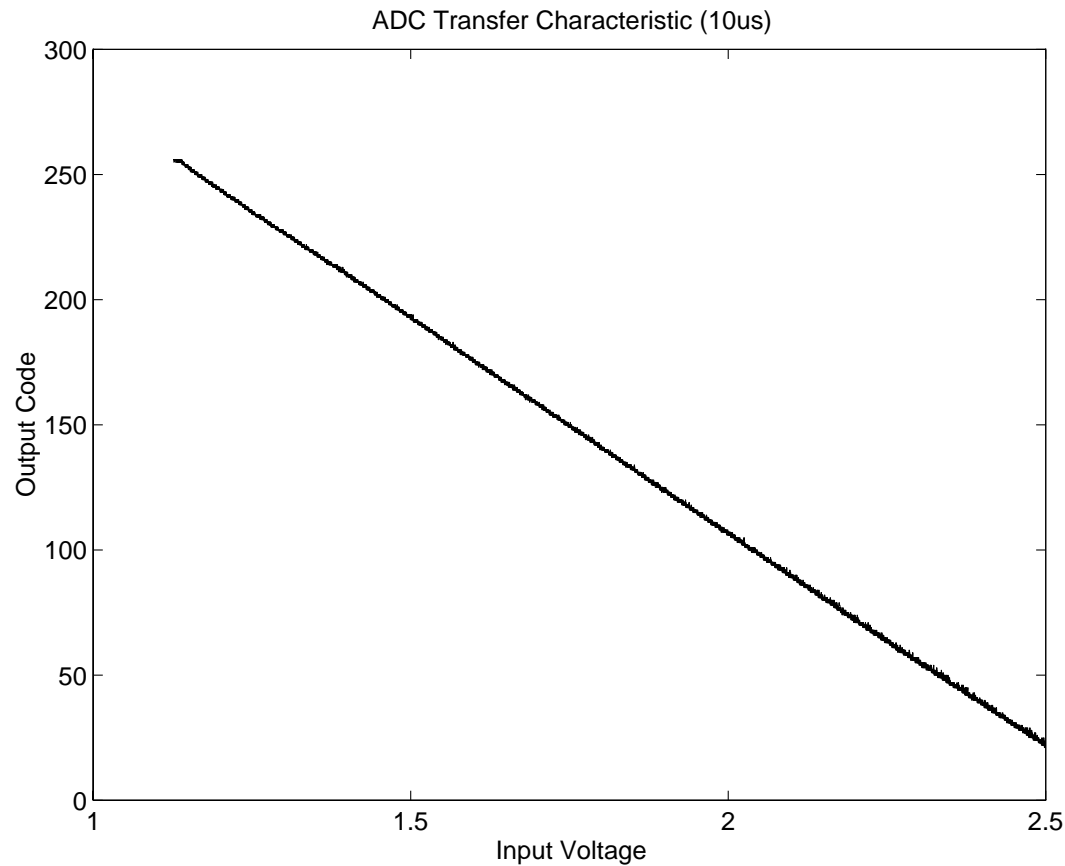


PIXEL
OUTPUT



SNR = 43dB with OSR = 64, Gain FPN = 1%

Measured MCBS ADC Transfer Function



**INL = 2.3 LSB, DNL = 1.2 LSB, Gain FPN = 0.24%,
and Offset FPN = 0.2%**

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Pixel Level ADC Comparison

	$\Sigma\Delta$ ADC	MCBS ADC
Size	4.25 transistors per pixel	4.5 transistor per pixel
Conversion mode	Charge to bits	Voltage to bits
Charge handling Capacity	Large	Small
FPN	Moderate	Small
Transistor noise sensitivity	Small	Moderate
Date rate	Large	Small
Quantization	Nonuniform – fixed by L	Programmable
External processing	Decimation Filtering	None
Required memory	Large	Small
Power Dissipation	Moderate	Small

Conclusions

- $\Sigma\Delta$ ADC is better suited to IR sensors
 - Large charge handling capacity
 - Fine quantization near the center of the range (i.e. small difference between large charge value can be determined)
- MCBS ADC is better suited to visible range sensors
 - Low output data rate
 - Programmable quantization
 - High sensitivity