# Quantitative Study of High Dynamic Range ΣΔ-based Focal Plane Array Architectures

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# Scene DR > FPA DR

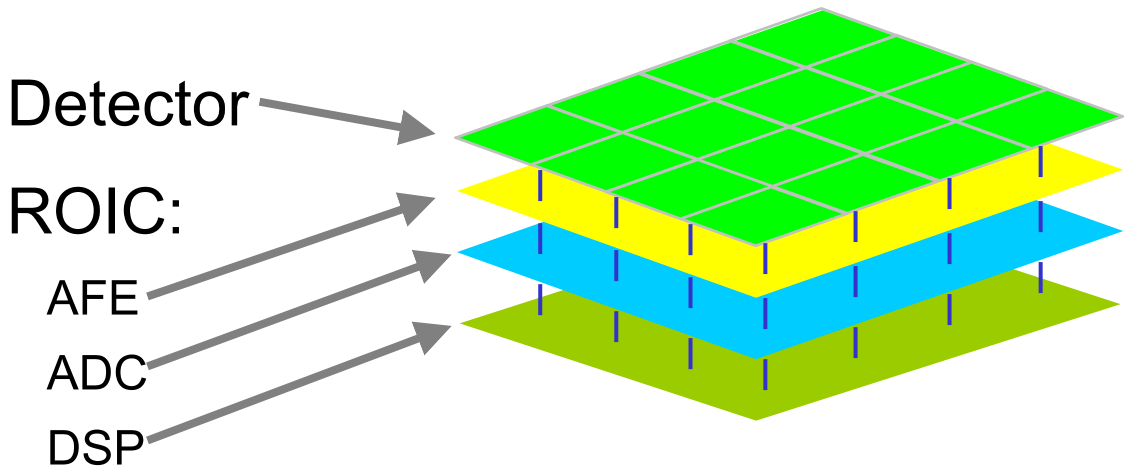


**Courtesy Pixim Corporation**

# DR Extension Methods

- Several methods have been developed to extend ROIC DR
- Implementation enabled by submicron CMOS and vertical integration
- Methods can be partially compared based on their SNR degradation [Yang `99, El Gamal `02]:
  - Some schemes extend DR but at expense of SNR degradation
- In previous paper we studied four such schemes [Kavusi `04]:
  - Time-to-saturation [Stoppa `02]
  - Multiple-capture [Yang `99]
  - Asynchronous self-reset with multiple capture [Liu `03]
  - Synchronous self-reset with residue readout [Rhee `03]

# Vertically Integrated Sensor Arrays




## Requirements

1. 25μm×25μm to 40μm×40μm
2. 1000 Frames/sec
3. 120dB dynamic range
4. 500mW/layer for 256 x 256 array

## Previous Study [Kavusi `04]

- Among all schemes studied in [Kavusi `04] only *synchronous self-reset with residue readout* achieves the requirements but has unacceptable fidelity

# The Two Presentations

- This presentation: Study extended counting scheme (based on $\Sigma\Delta$ modulator) [Jansson `95]
  - ✓ Show that it can achieve the DR and frame rate requirements with high fidelity
  - ✗ Power consumption can be high

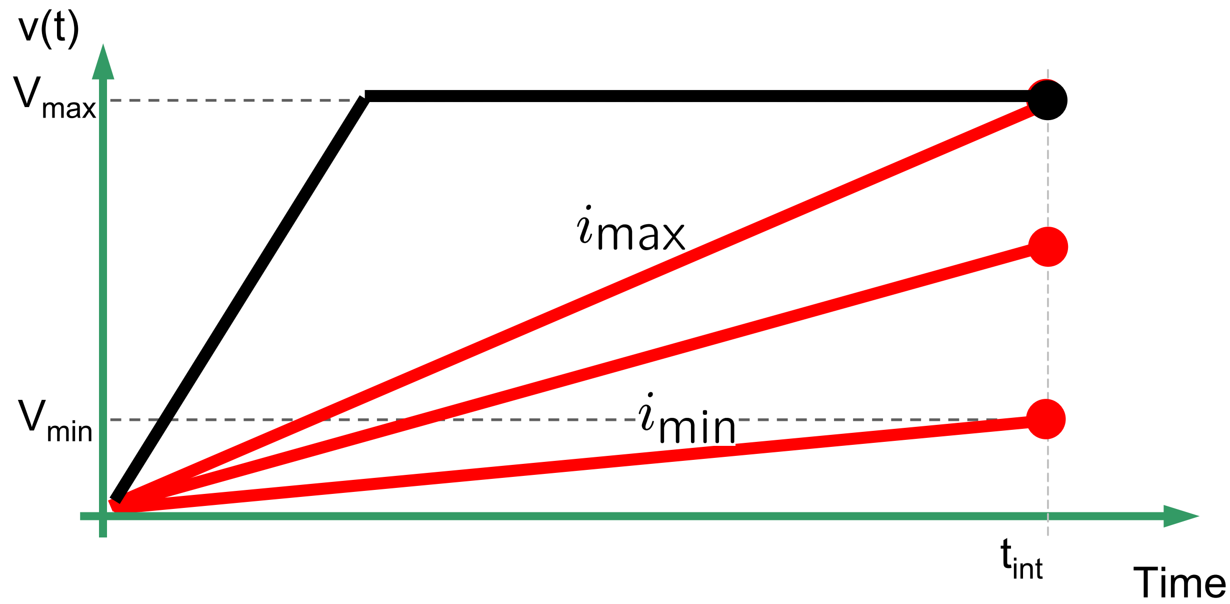
✓ The next presentation: We describe a new scheme that can satisfy *all VISA* requirements

# Outline

- Conventional sensor DR and SNR
- 1-bit incremental ΣΔ [Fowler `94]
- Extended counting [Jansson `95]
- Power consumption estimate

# Conventional (Reference) Sensor

- CTIA, CCD, APS

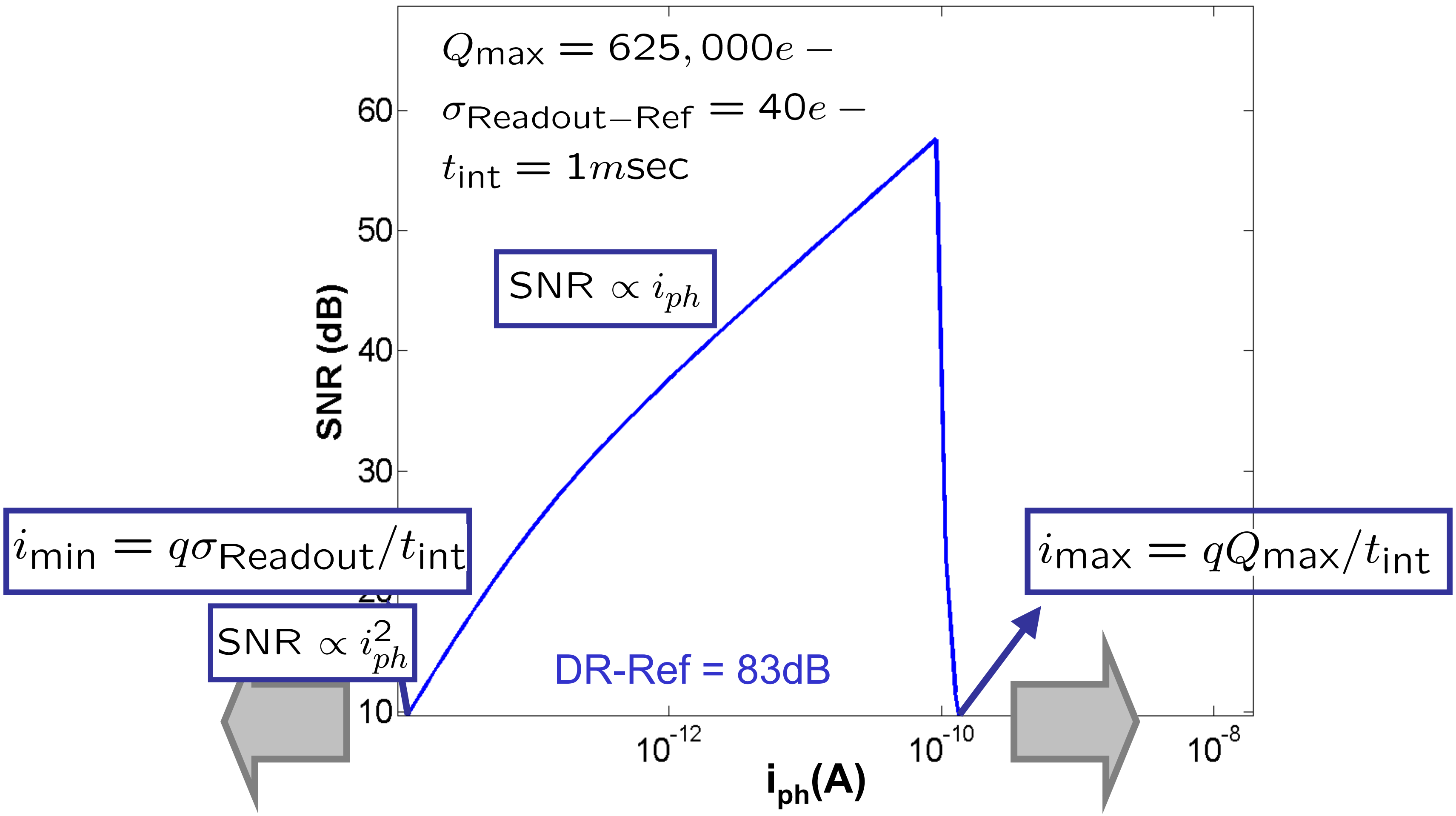



$$\mathrm{DR} = i_{\mathrm{max}}/i_{\mathrm{min}}$$

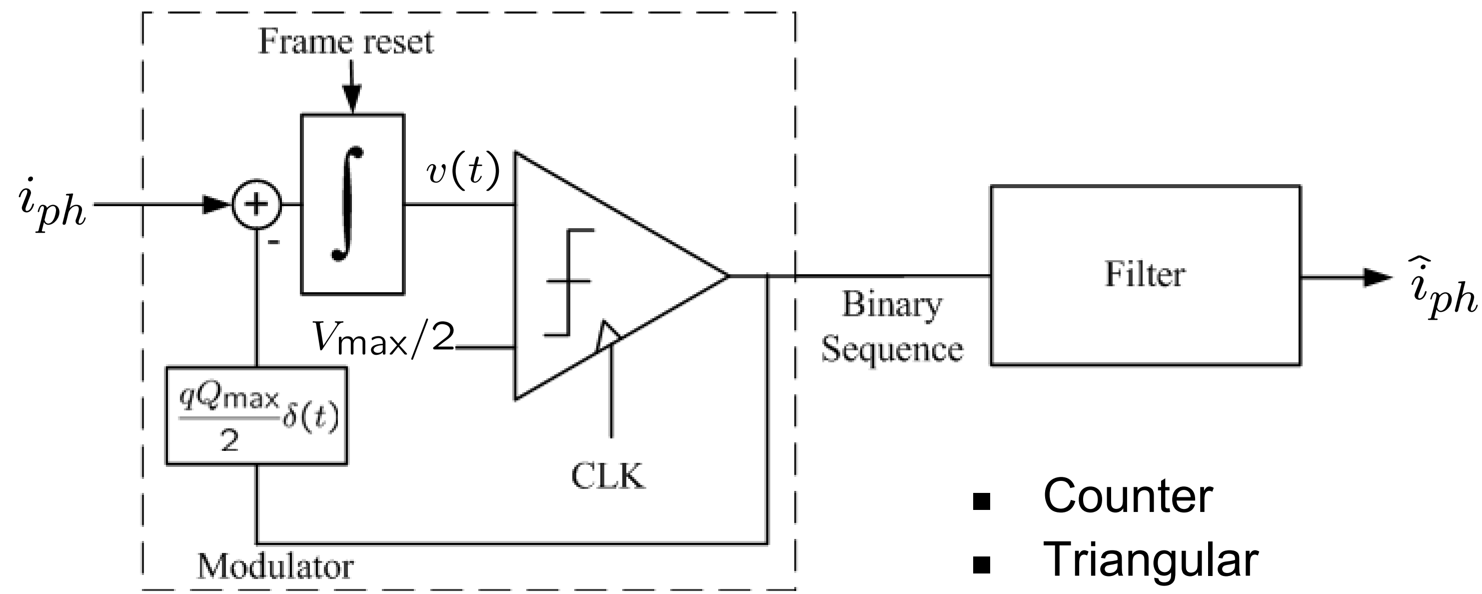
$$i_{\mathrm{min}} = q\sigma_{\mathrm{Readout}}/t_{\mathrm{int}} \qquad i_{\mathrm{max}} = qQ_{\mathrm{max}}/t_{\mathrm{int}}$$

# Conventional (Reference) Sensor

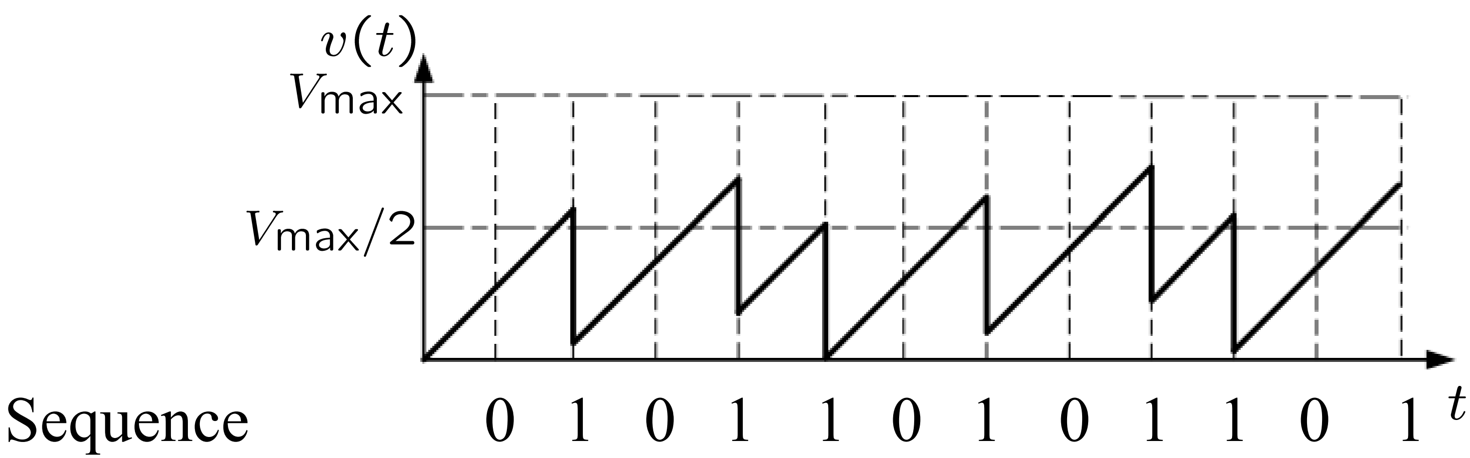
- CTIA, APS, CCD



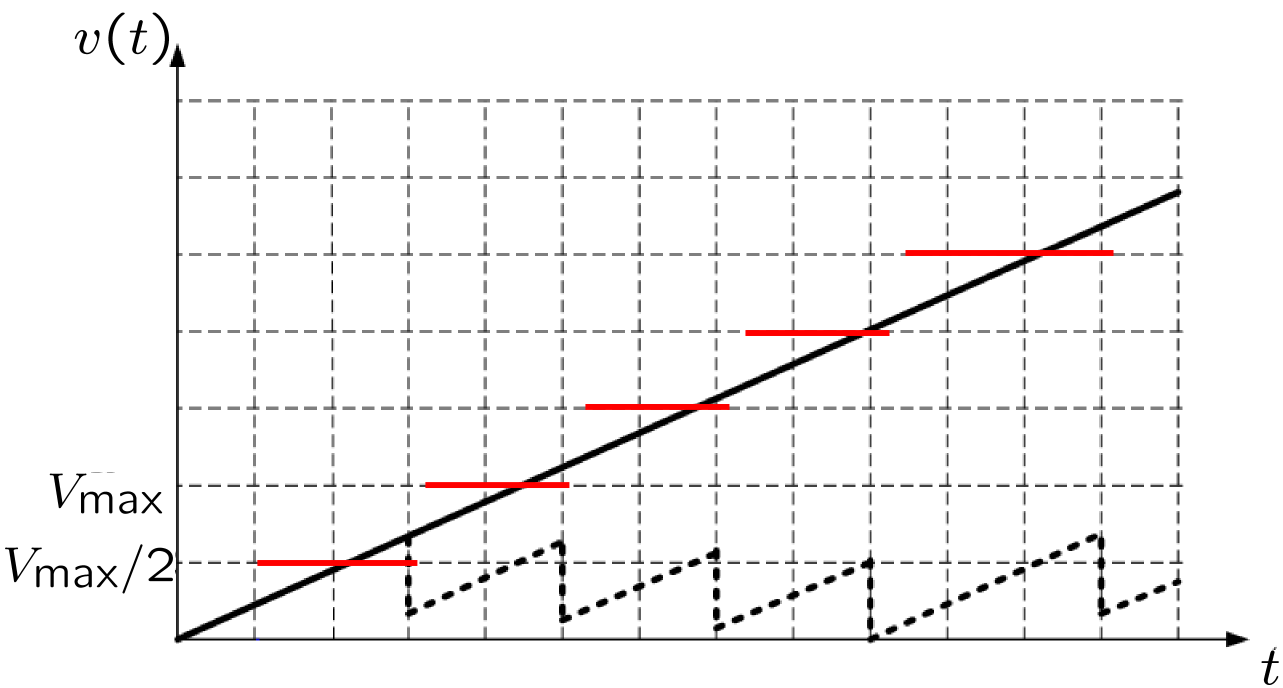
# 1-bit Incremental ΣΔ Modulator [Fowler `94]




- Counter
- Triangular
- Zoomer, recursive

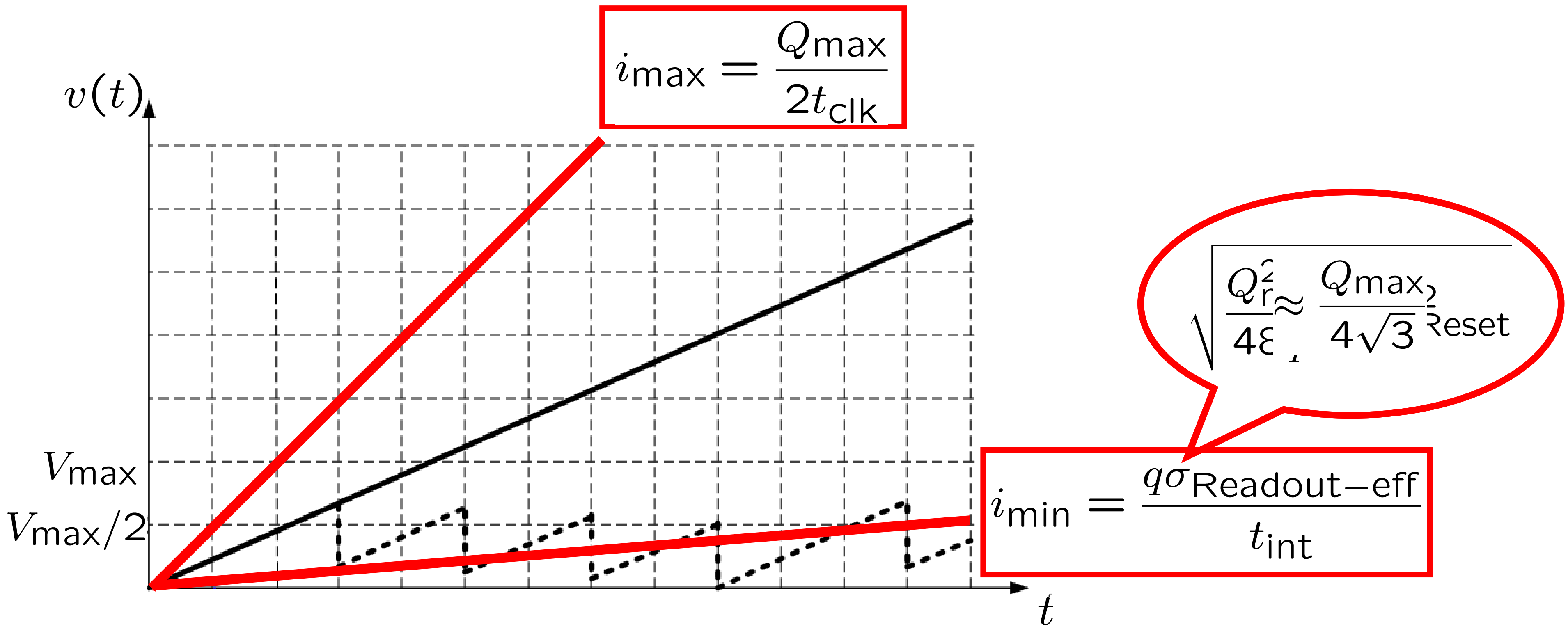


# Equivalent Ramp

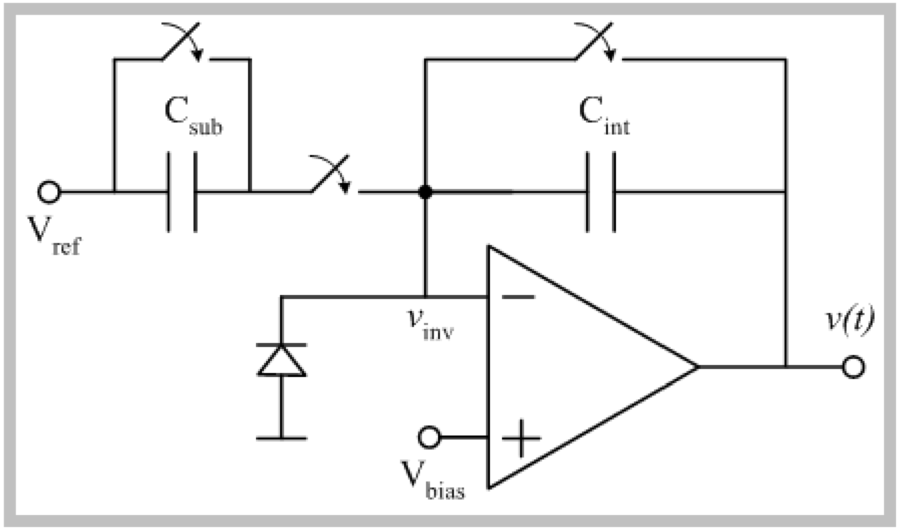



| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sequence | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | |
| Threshold | 1 | 1 | 1 | 2 | 2 | 3 | 3 | 4 | 4 | 5 | 5 | 5 | 6 | (x $V_{max}/2$) |

# Dynamic Range

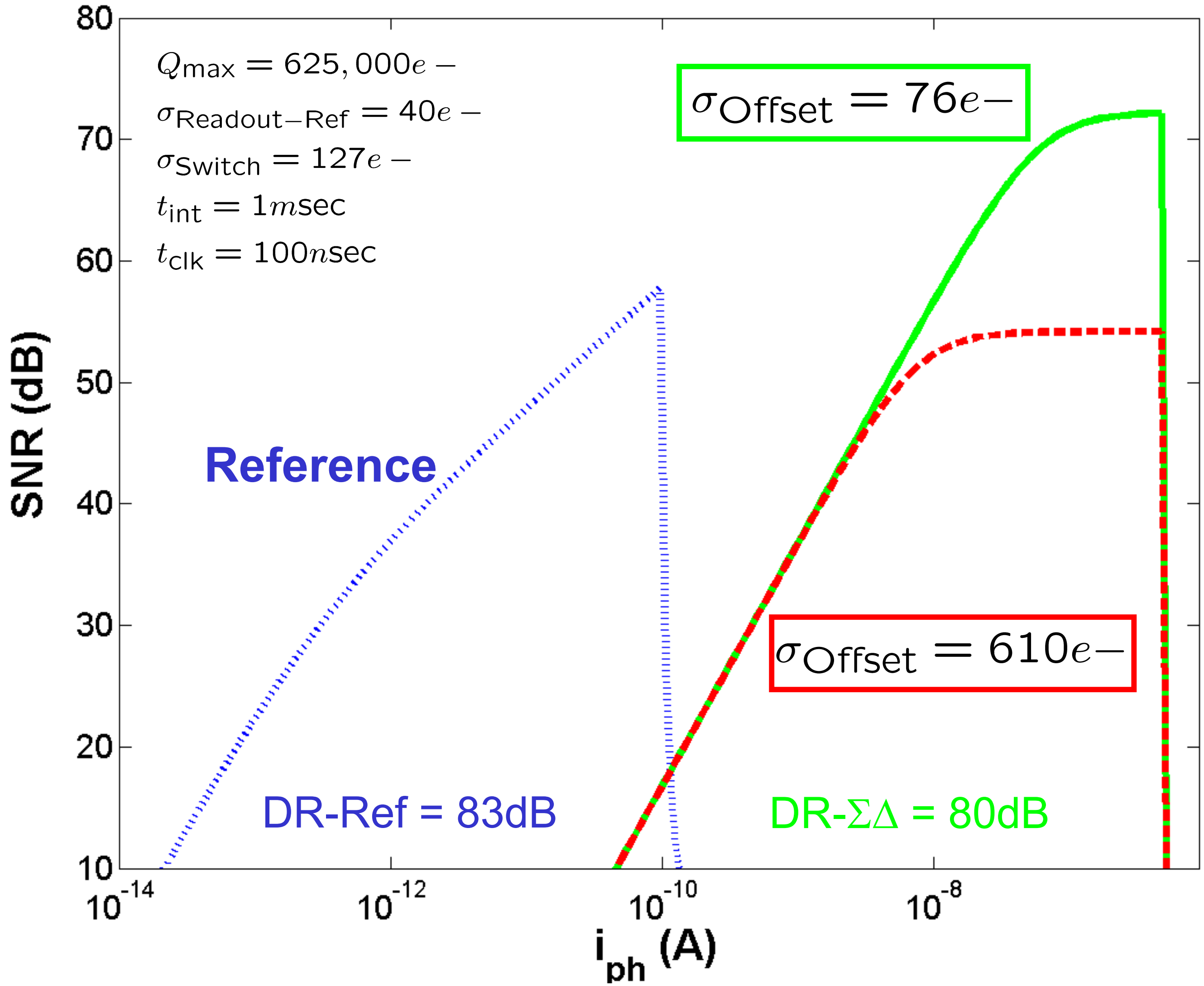


# 1-bit Incremental ΣΔ Modulator [Fowler `94]



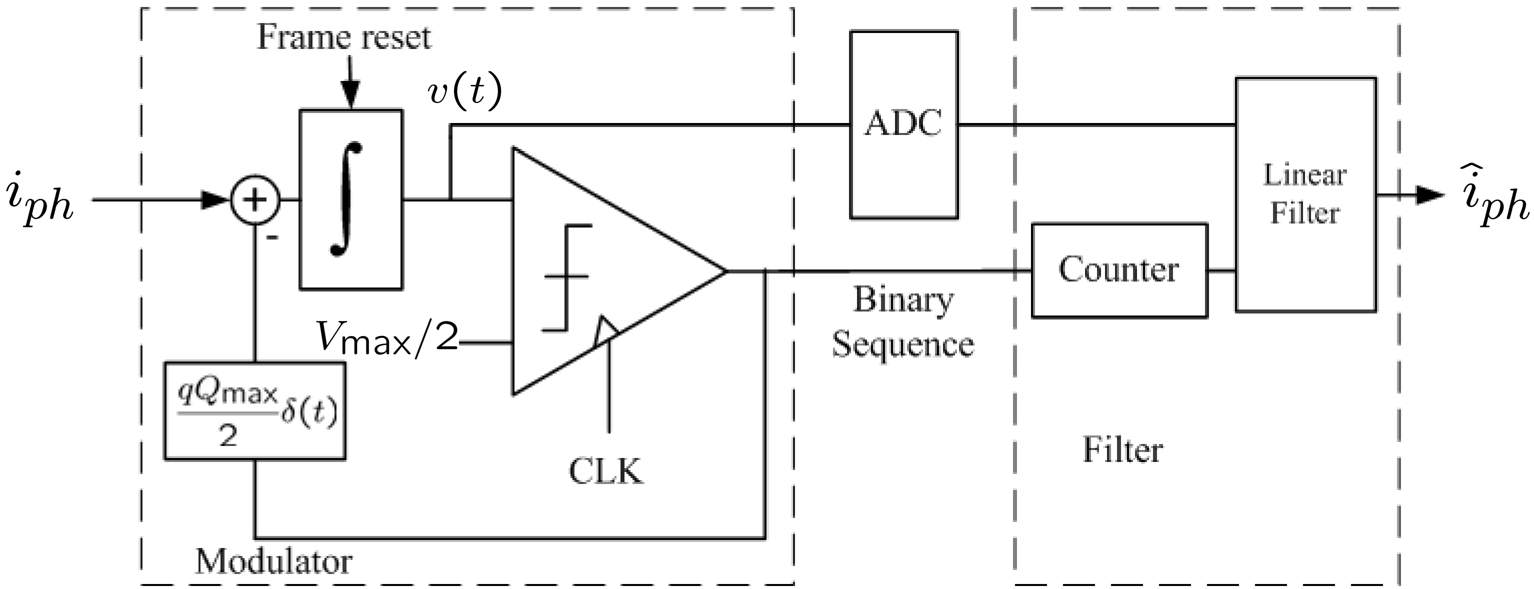

- High end limited by subtraction mismatch
  - Due to capacitor mismatches, pedestal error variation, reference voltage variation, settling time variation, finite dc gain -- represented by $\sigma_{Offset}$
  - ✘ $\sigma_{Offset}$ accumulates → gain fixed pattern noise

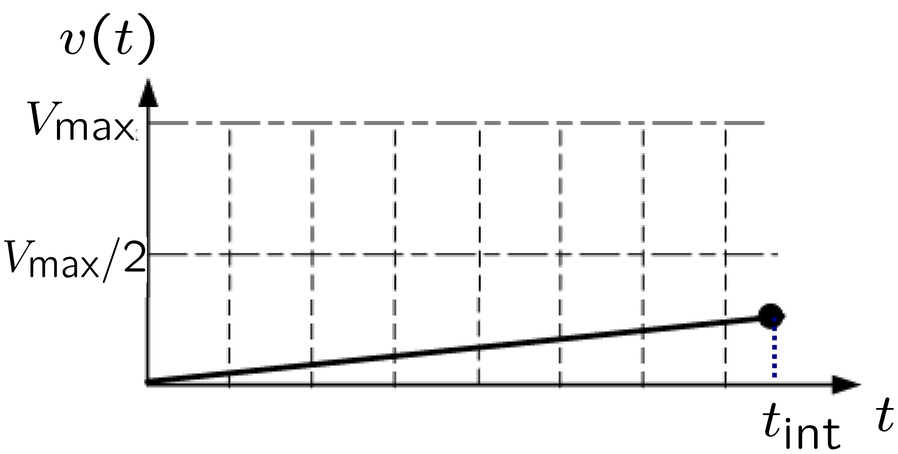
# SNR

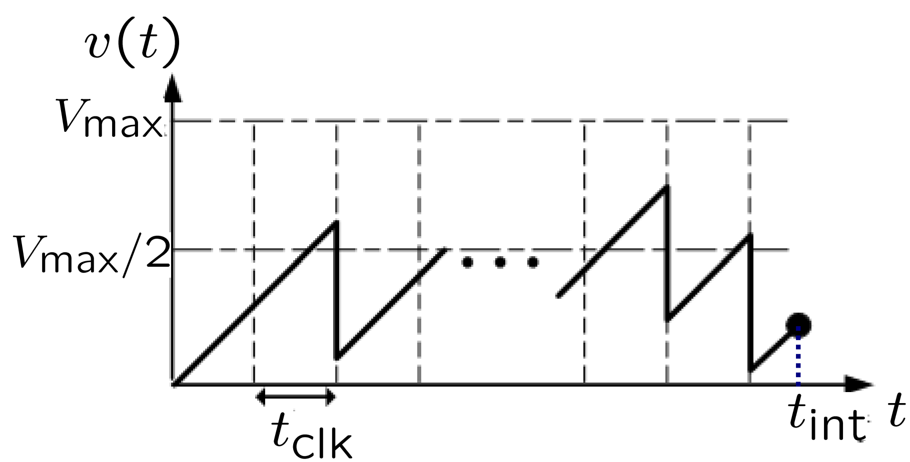


$Q_{\text{max}} = 625,000e-$
$\sigma_{\text{Readout-Ref}} = 40e-$
$\sigma_{\text{Switch}} = 127e-$
$t_{\text{int}} = 1m\text{sec}$
$t_{\text{clk}} = 100n\text{sec}$
$\sigma_{\text{Offset}} = 76e-$
$\sigma_{\text{Offset}} = 610e-$
Reference
DR-Ref = 83dB
DR-ΣΔ = 80dB
SNR (dB)
80
70
60
50
40
30
20
10
$10^{-14}$
$10^{-12}$
$10^{-10}$
$10^{-8}$
$i_{ph}$ (A)

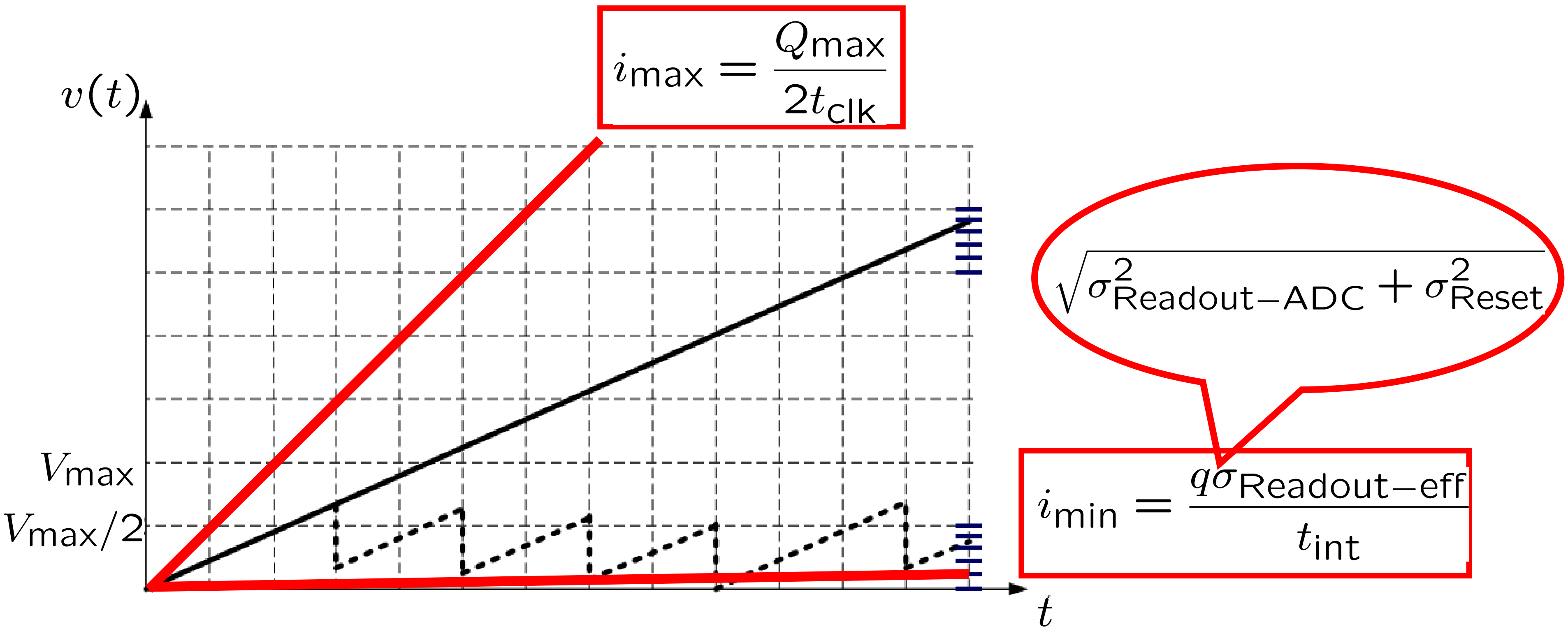
# Extended Counting [Jansson `95]



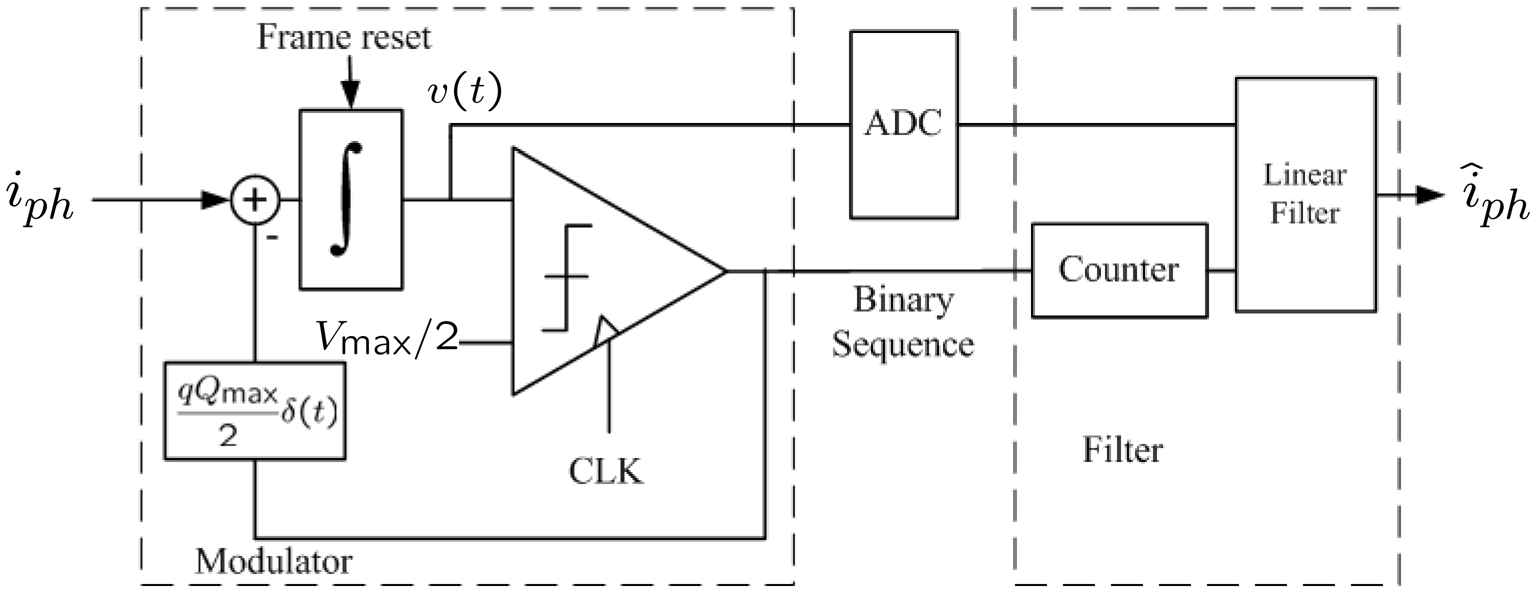



# Dynamic Range

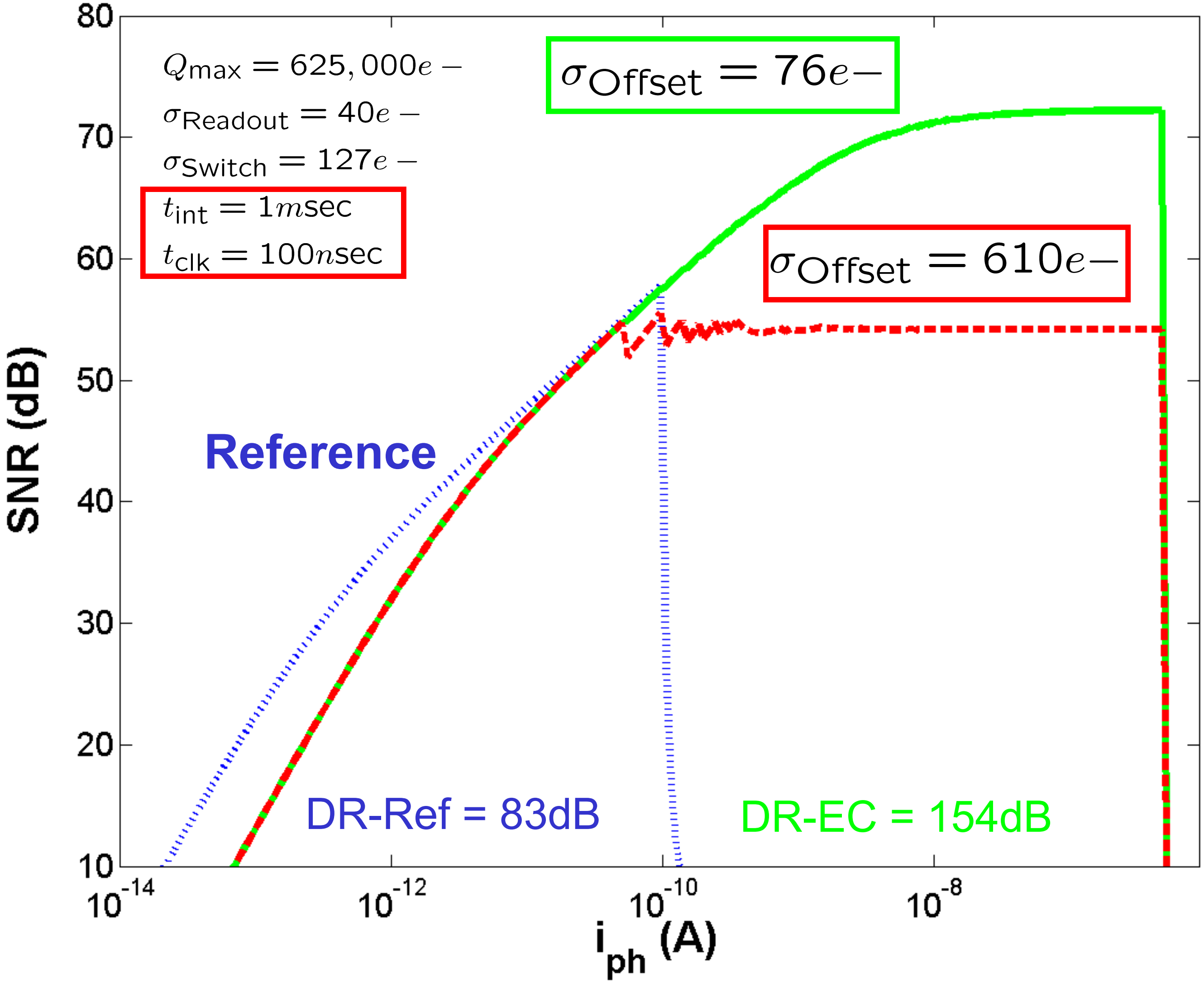


# Extended Counting [Jansson `95]




- Low end limited by reset noise
- High end limited by subtraction mismatch -- same as 1-bit ΣΔ

# SNR



80
70
60
50
40
30
20
10
SNR (dB)
$Q_{\text{max}} = 625{,}000e-$
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$t_{\text{int}} = 1m\text{sec}$
$t_{\text{clk}} = 100n\text{sec}$
$\sigma_{\text{Offset}} = 76e-$
$\sigma_{\text{Offset}} = 610e-$
Reference
DR-Ref = 83dB
DR-EC = 154dB
$10^{-14}$
$10^{-12}$
$10^{-10}$
$10^{-8}$
$i_{ph}$ (A)

# Power Consumption Estimate

- Power consumption for a 256 x 256 FPA employing extended counting at 1000 fps and 120dB DR
- View the whole ROIC as a data converter
- Assume FoM = Power/($2^{bits}$x2BW) = 0.5pJ (aggressive) [Walden '99]
- Extended counting yields uniform quantization
  - 120dB = 20-bit of resolution
- Power estimate = 0.5p x $2^{20}$ x 1000 x $256^2$

  = 34Watt

# Conclusion

- Extended counting achieves the VISA DR and speed requirements with good fidelity
  - Limited by reset noise and charge subtraction accuracy
- Extended counting is a uniform quantizer → high power consumption
  - For the high dynamic range high frame rate requirements

# SNR (optimal filter)