EXPERIMENTAL HIGH SPEED CMOS IMAGE SENSOR SYSTEM & APPLICATIONS

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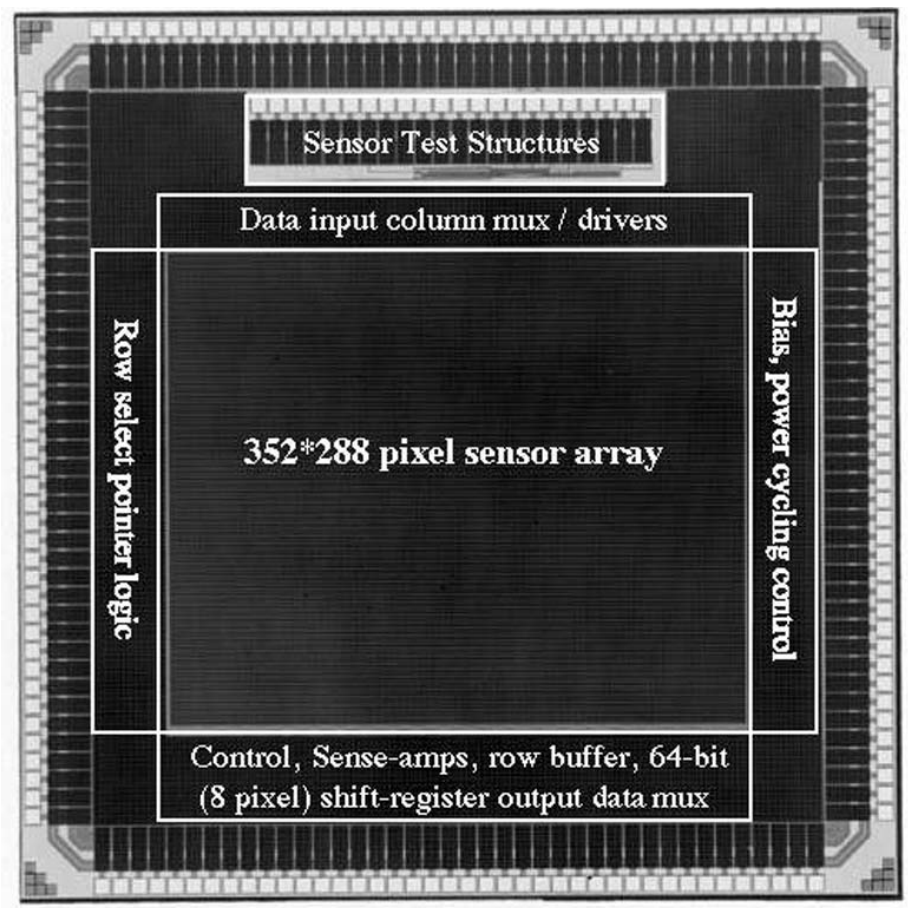
Background

- CMOS image sensors offer:
  - Low cost and low power consumption
  - High frame rate non-destructive readout
  - Integration of capture with analog and digital signal processing on same chip
- Enable novel still and video rate imaging applications:
  - Dynamic range extension (Liu SPIE'01, Yang JSSC'99)
  - Motion-blur prevention (Liu ICASSP'01)
  - Accurate optical flow estimation (Lim ICIP'01)
  - Gain FPN reduction (Lim SPIE'02)

Motivation and Outline

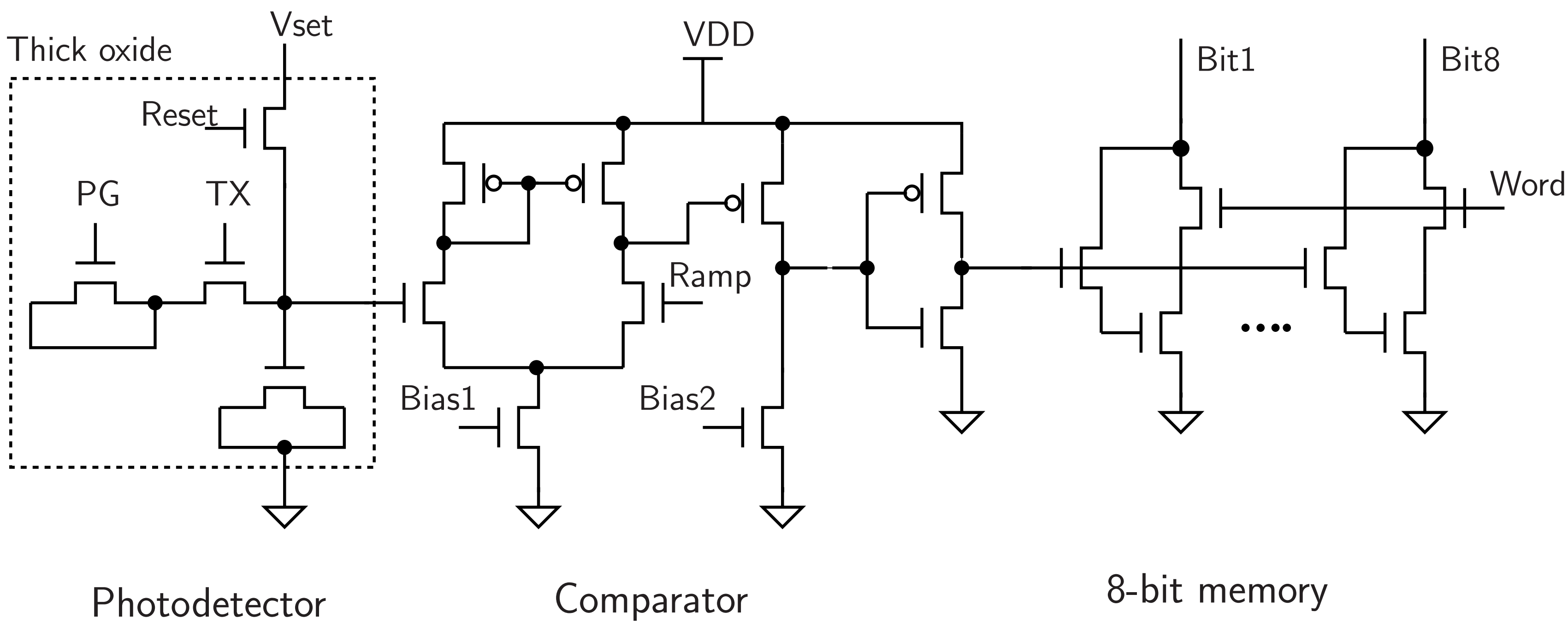
- Our group designed a 10,000 frames/s CMOS Digital Pixel Sensor (DPS) chip (Kleinfelder JSSC'01)
- We designed a PC based imaging system around this chip to explore these high frame rate applications
- Outline:
  - Describe the DPS chip
  - Describe the high speed system
  - Examples of the applications

10,000 frames/s DPS Chip (Kleinfelder JSSC'01)



- 0.18μm CMOS digital technology
- 352×288 pixels (CIF)
- $9.4\mu \times 9.4\mu$ pixels
- 8 bit single slope ADC and memory/ pixel
- Integrated clock distribution, gray code counter, power cycling control
- 64 bit digital output bus

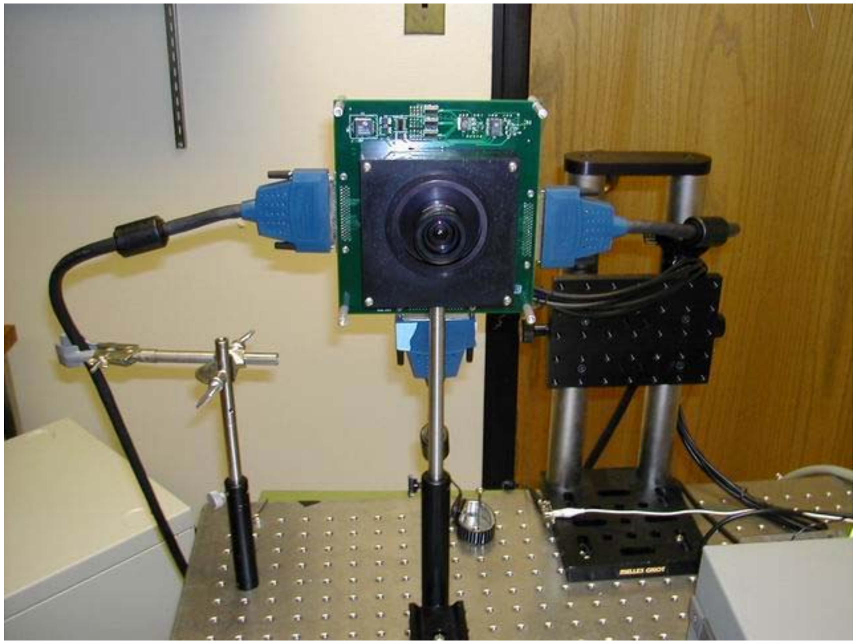
DPS Pixel

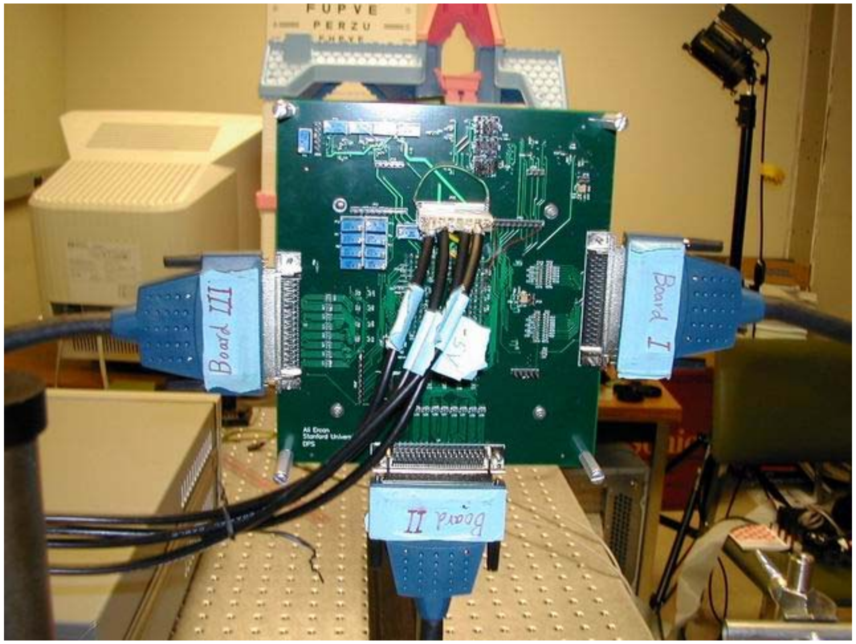


Thick oxide
Vset
Reset
PG
TX
VDD
Ramp
Bias1
Bias2
Bit1
Bit8
Word
....
Photodetector
Comparator
8-bit memory

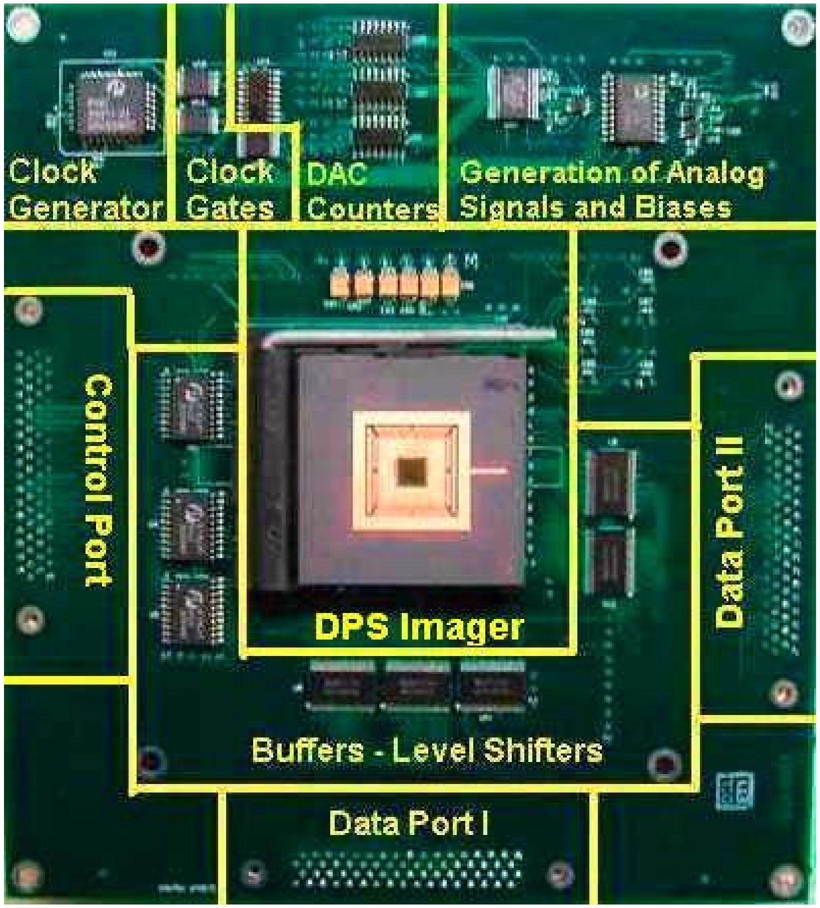
High Speed CMOS Imaging System

- Built around the DPS chip
- Interfaced to PC
- Programmable via Matlab interface
- Runs up to 1,400 frames/s



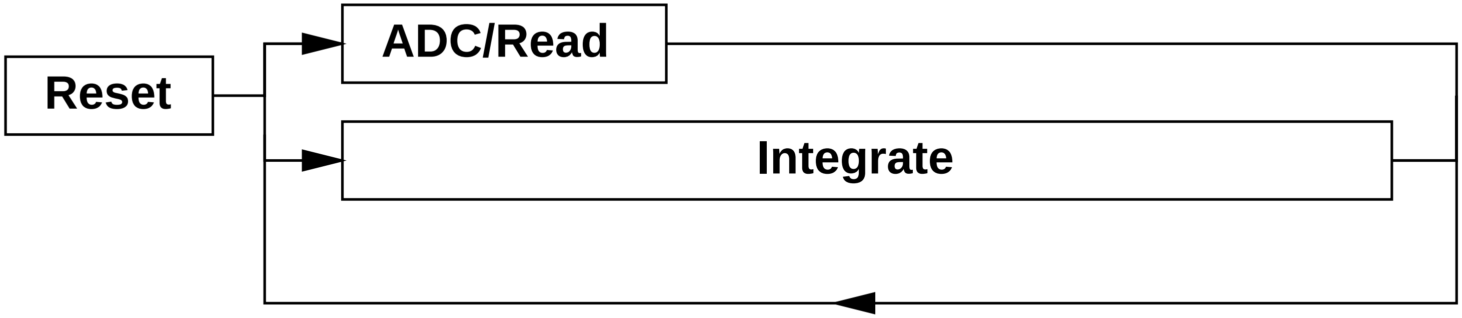


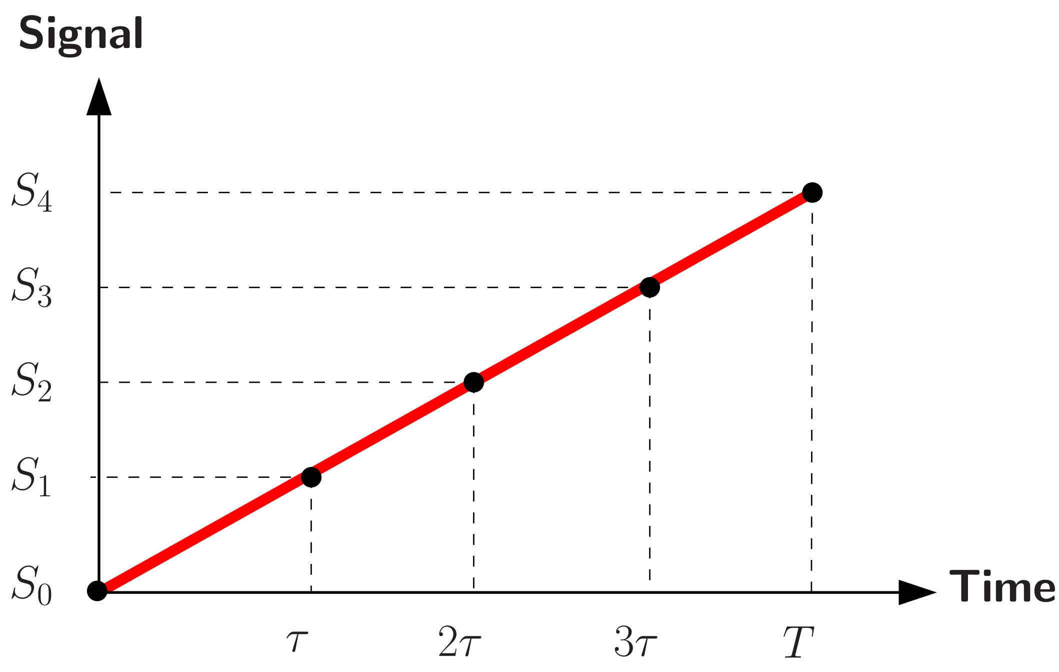
The PCB



Clock Generator
Clock Gates
DAC Counters
Generation of Analog Signals and Biases
Control Port
DPS Imager
Data Port II
Buffers - Level Shifters
Data Port I

Multiple Non-destructive Capture Mode





Imaging High Dynamic Range Scene

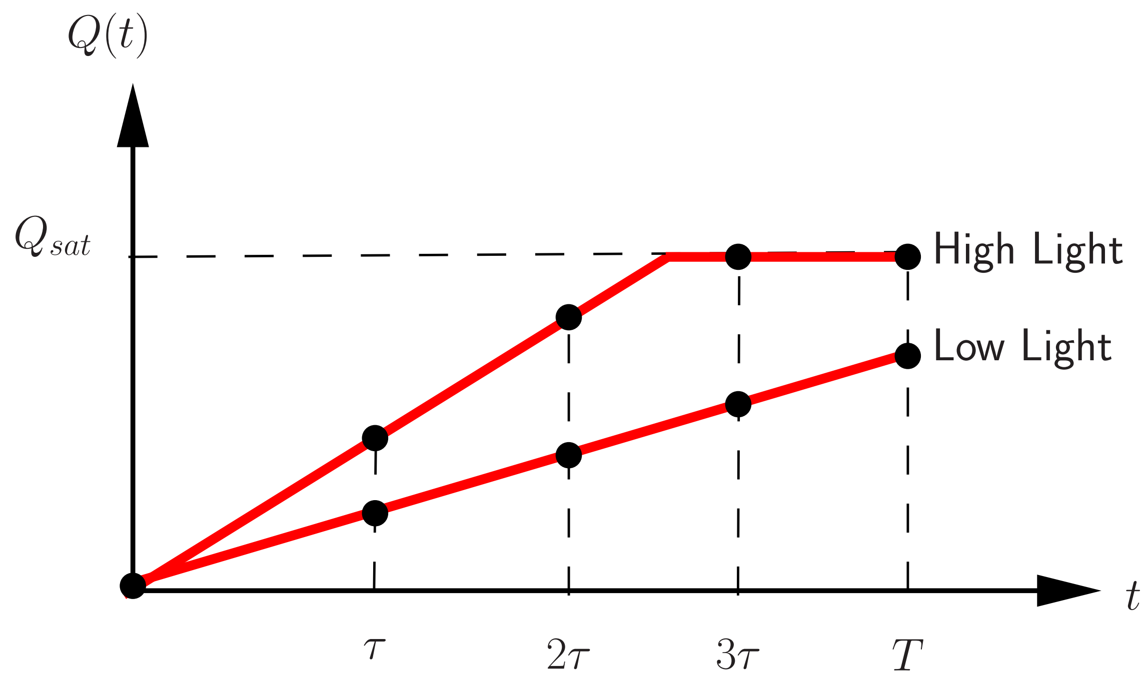
Short Exposure-time Image

Medium Exposure-time Image

Long Exposure-time Image

Application: Dynamic Range Extension

- Capture multiple images non-destructively
- Last-Sample-Before-Saturation Algorithm(Yang JSSC'99): For each pixel use an appropriately scaled version of its last sample before saturation



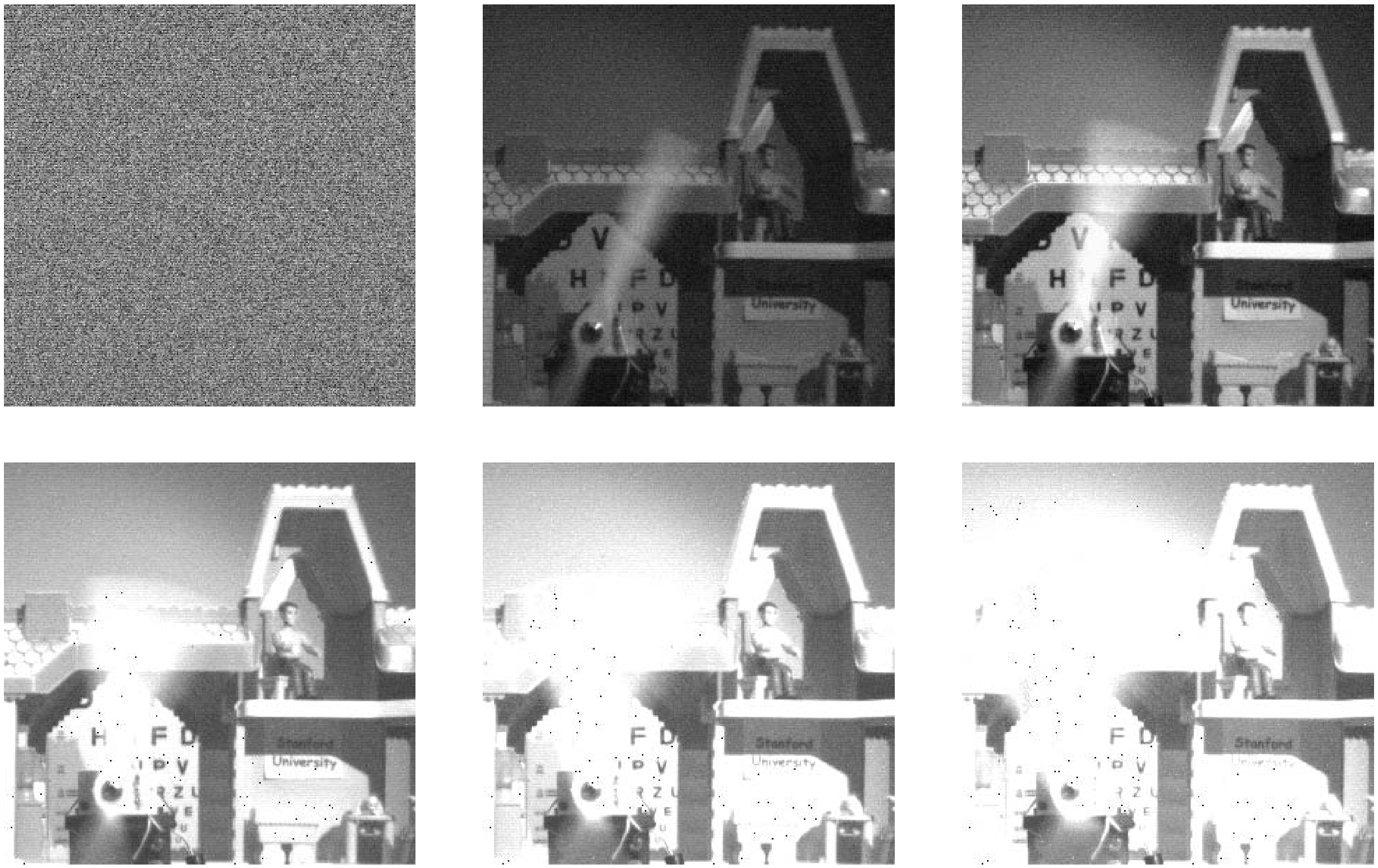
- Only extends dynamic range at high illumination

Extending Dynamic Range at Low Illumination

- Need to increase SNR for low illumination signals
- Making exposure time longer increases SNR but can cause motion blur
- Developed two pixel-wise techniques:
  - Reduce read noise using weighted average of samples before saturation (Liu SPIE'01)
  - Prevent image blur by detecting motion (Liu ICASSP'01)

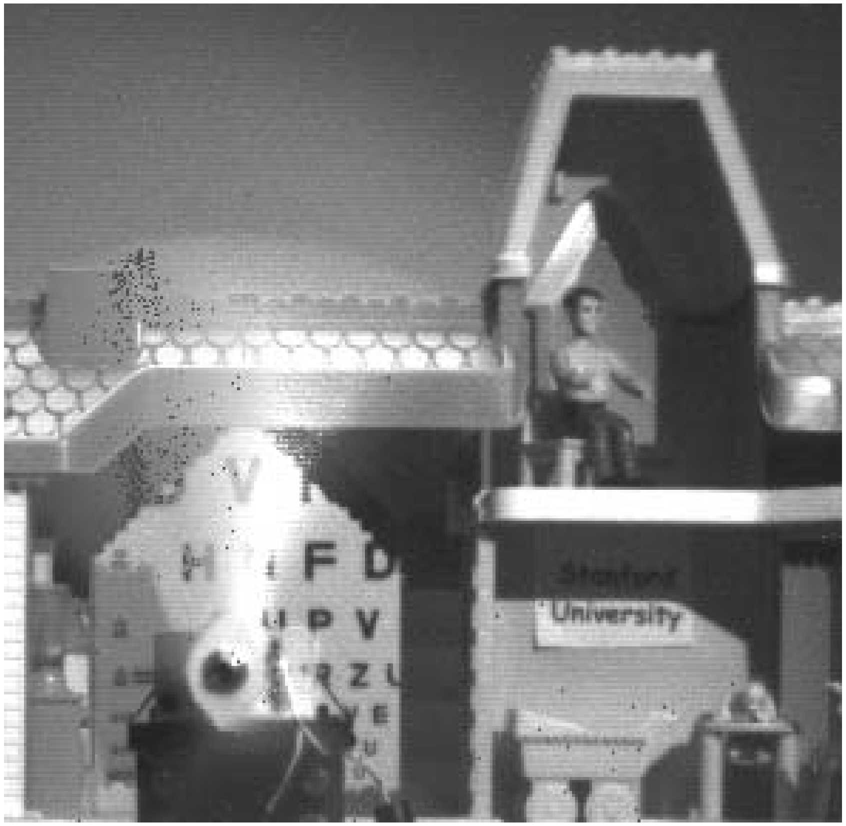
65 Image Capture Example

0ms 10ms 20ms

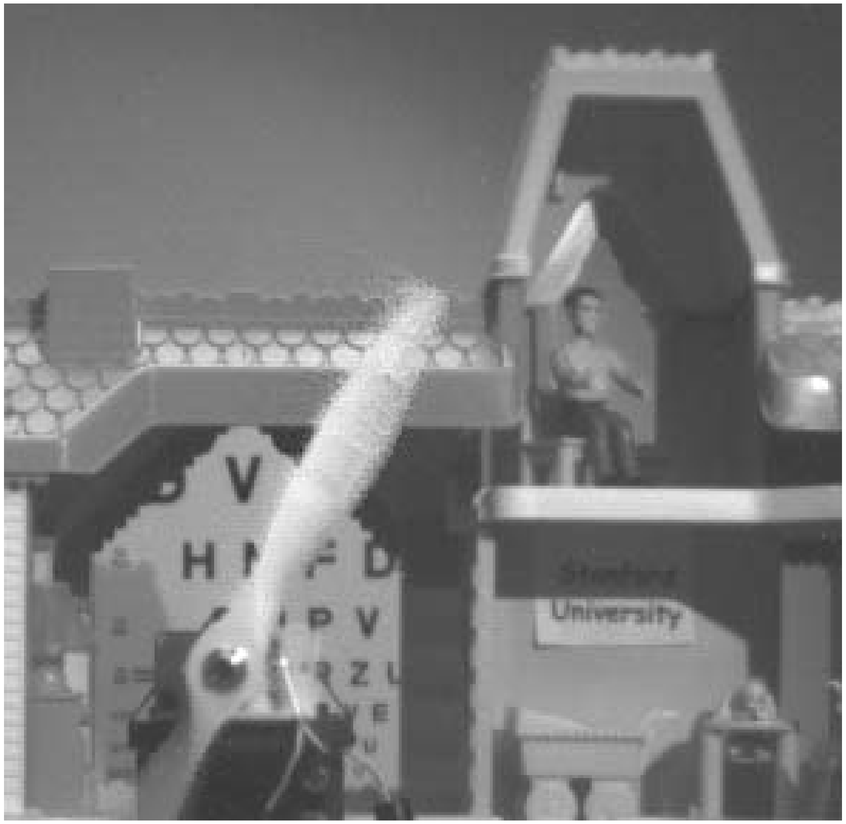


30ms 40ms 50ms

High Dynamic Range Images

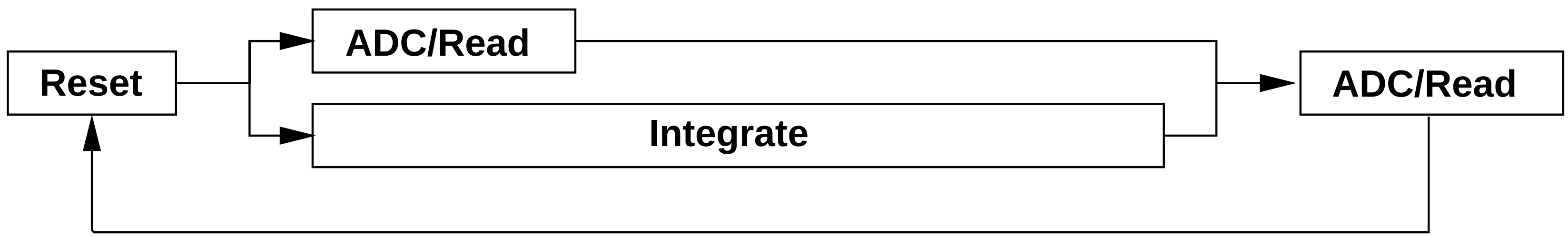


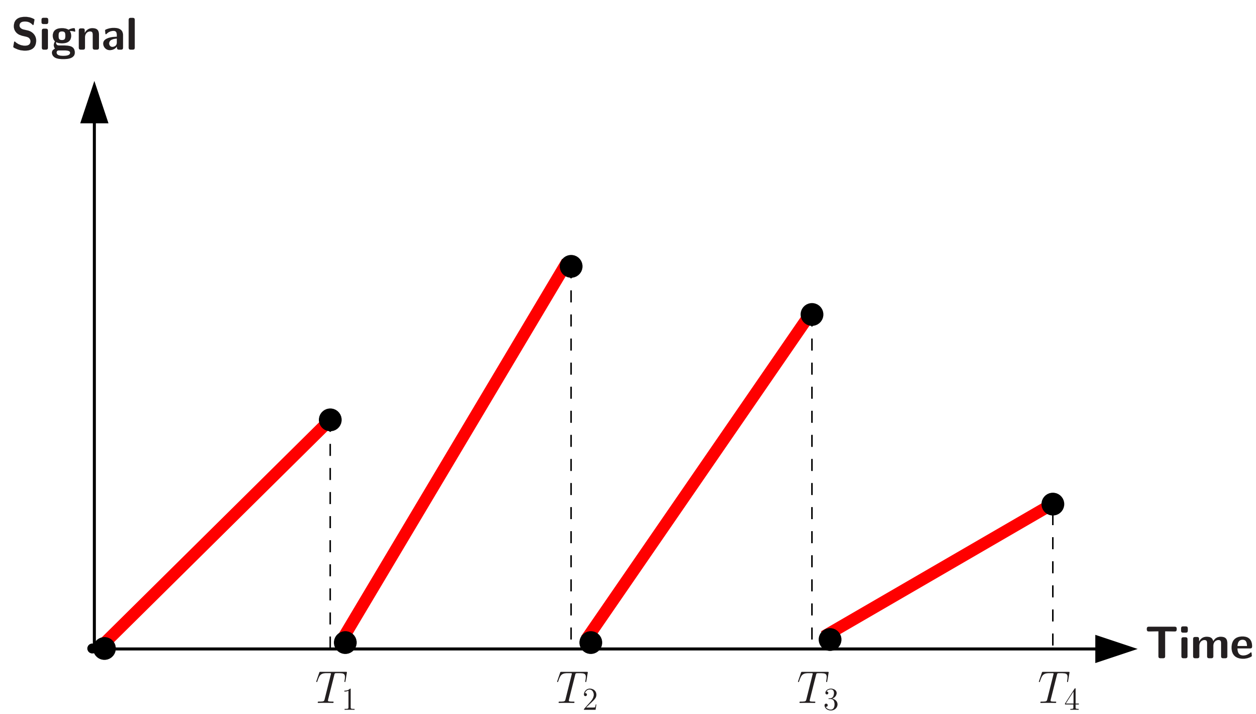
LSBS



Estimation and motion-blur prevention

Video Mode with Digital CDS



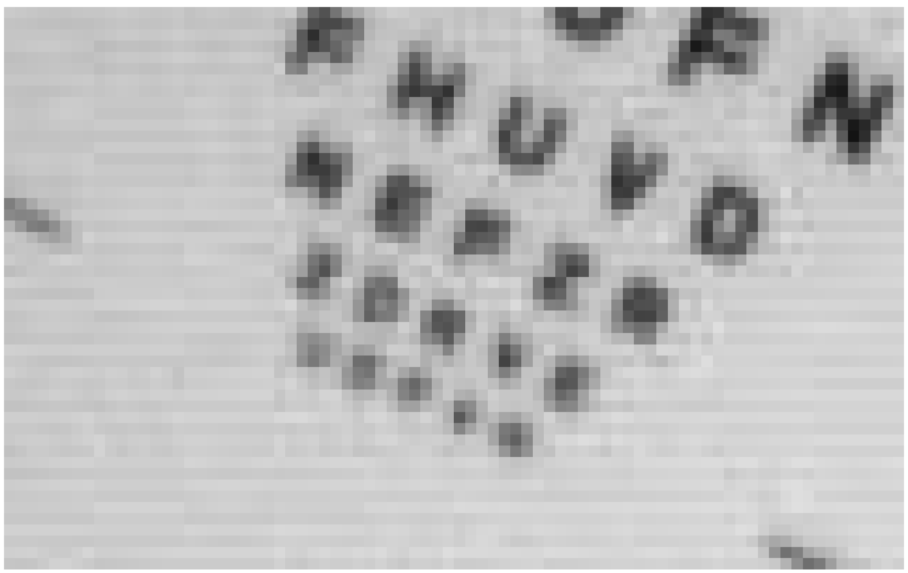


Application: Optical Flow Estimation

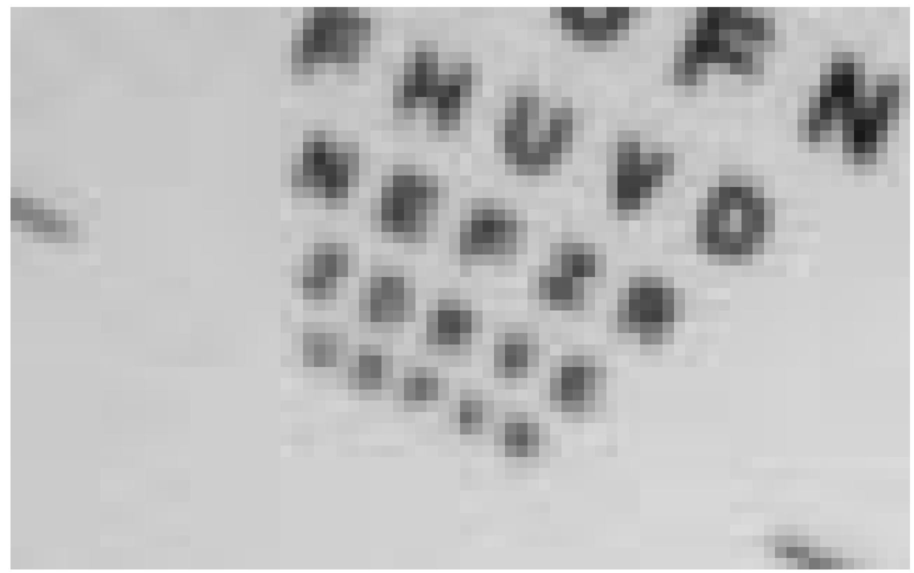
- Optical flow estimation is basis for *many* video applications
- Many of these applications need accurate optical flow estimation
- Using high frame rate sequence, we developed method for accurately estimating optical flow at standard frame rate (Lim ICIP'01)
- Application: Sensor gain Fixed Pattern Noise (FPN) correction (Lim SPIE'02)
  - No existing method for gain FPN correction
  - CDS only removes offset FPN

Gain FPN Correction Example

- Captured 5 frames of eye chart at 200 frames/s using our system
- Used sequence and its optical flow to correct gain FPN



Before FPN Correction



After FPN Correction

Conclusion

- Described experimental high speed CMOS imaging system based on 10,000 frames/s DPS chip
- Used system to demonstrate high frame rate applications to
  - Still imaging: Dynamic range extension and motion blur prevention via multiple non-destructive captures
  - Video-rate imaging: Optical flow estimation and gain FPN correction

DPS Chip Characteristics (Kleinfelder JSSC'01)

Technology	0.18μm 5-metal CMOS
Die size	5$\times$5 mm
Array size	352$\times$288 pixels
Number of transistors	3.8 million
Readout architecture	64-bit (167 MHz)
Max output data rate	$>$1.33 GB/s
Max continuous frame rate	$>$10,000 frames/s
Max continuous pixel rate	$>$1 Gpixels/s
Pixel size	9.4μm$\times$9.4μm
Photodetector type	nMOS Photogate
Number of transistors/pixel	37
Sensor fill factor	15%

DPS Characterization Results (Kleinfelder JSSC'01)

Power used at 10K frames/s	50mW, typical
ADC architecture	Per-pixel single-slope
ADC resolution	8-bits
ADC conversion time, typical	$\sim$25μs, ($\sim$20μs, min.)
ADC range, typical	1V
ADC integral non-linearity	$<$0.22% (0.56 LSB)
Dark current (20^{o}C)	130mV/s, 10nA/cm^2
Quantum efficiency	13.6%
Conversion gain	13.1μV/e$^-$
Sensitivity	0.107V/lux.s