Folded Multiple-Capture:
An Architecture for High Dynamic Range Disturbance-Tolerant Focal Plane Array

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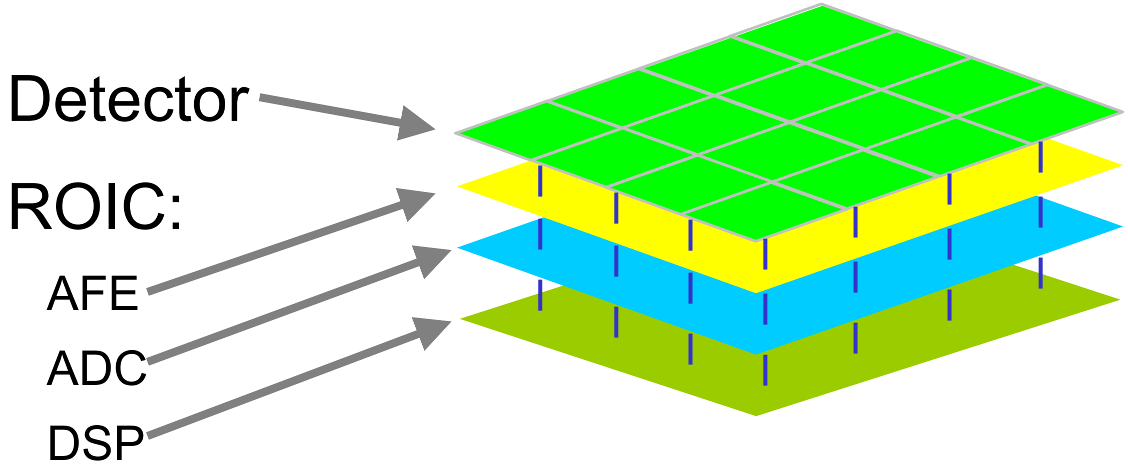
Vertically Integrated Sensor Arrays



Requirements

1. 25μm×25μm to 40μm×40μm
2. 1000 Frames/sec
3. 120dB dynamic range
4. 500mW/layer for 256 x 256 array

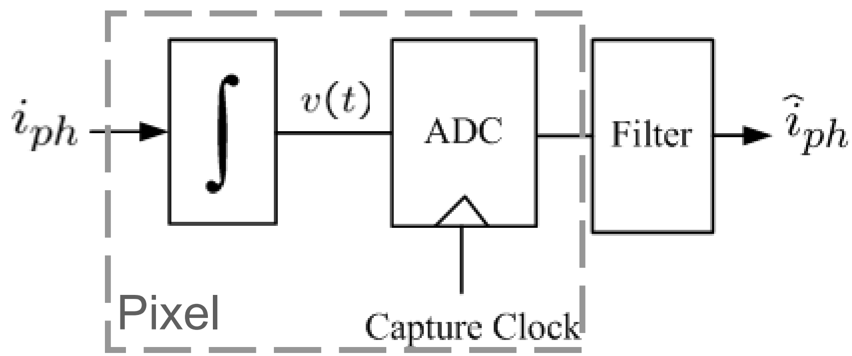
Previous Studies [Kavusi `04]

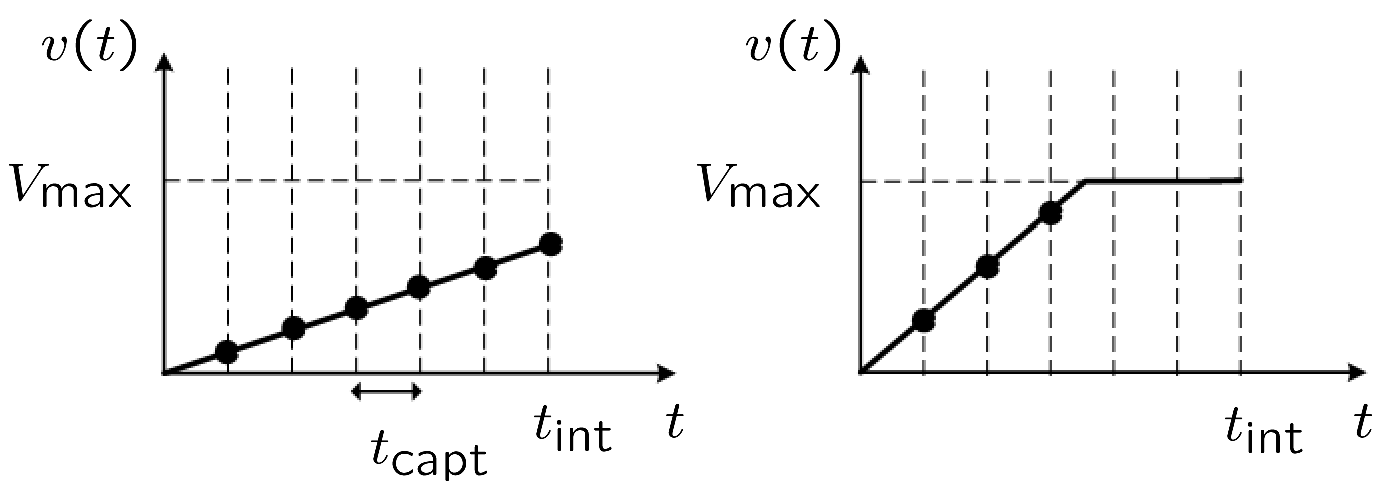
- ✘ None of the studied schemes can meet all VISA requirements with acceptable fidelity (SNR)
- ✓ We present new scheme that meets *all* the requirements

Outline

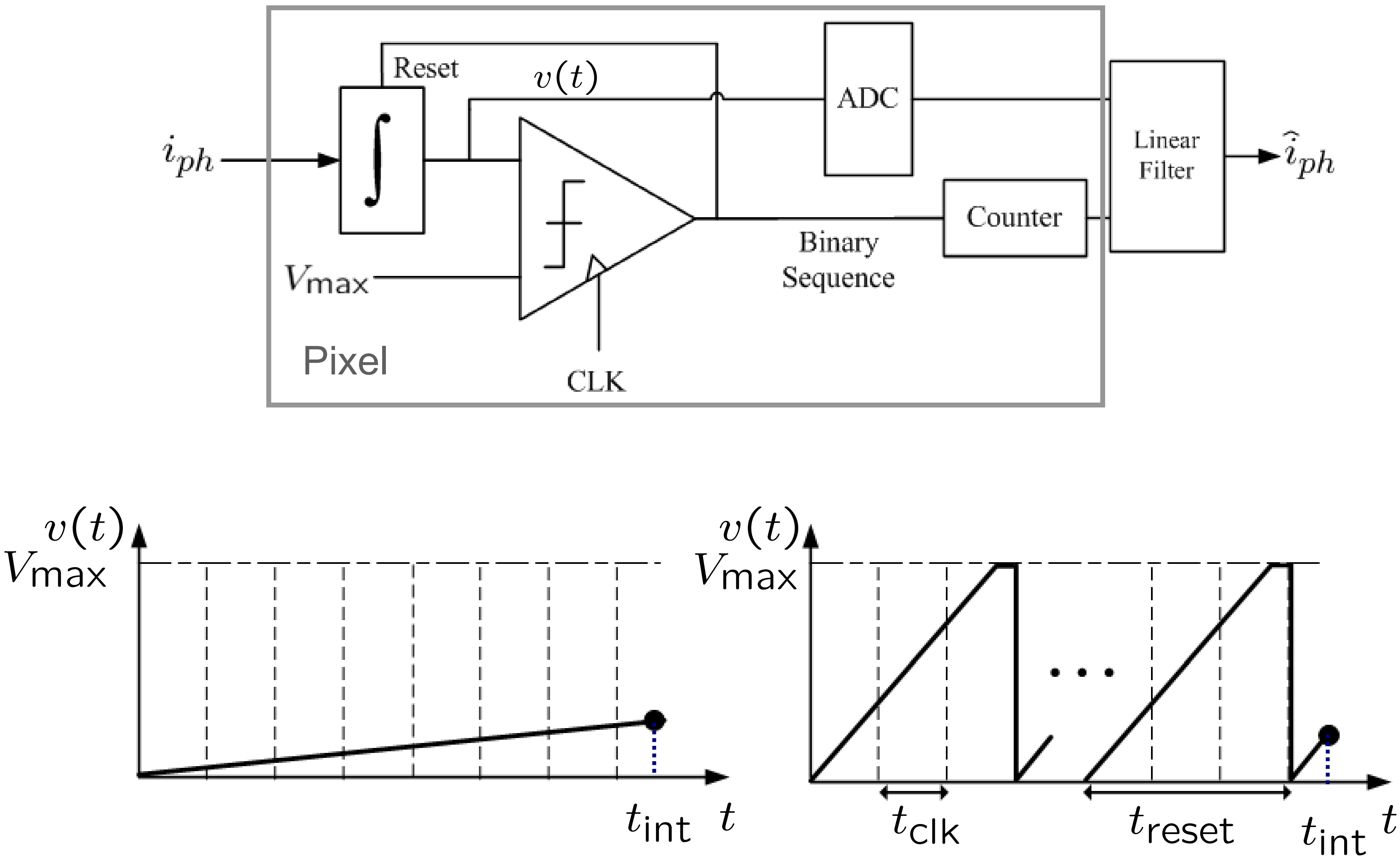
- Multiple-capture and Synchronous self-reset
- Folded Multiple Capture
- Disturbance Tolerance
- Comparison to Extended Counting

Multiple-Capture [Yang `99]





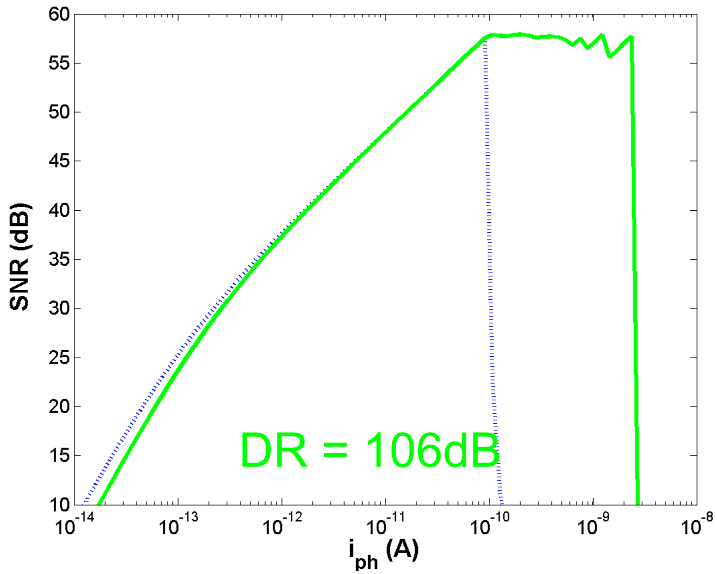
Synchronous Self-Reset [Rhee `03]



Summary of The Two Schemes [Kavusi `04]

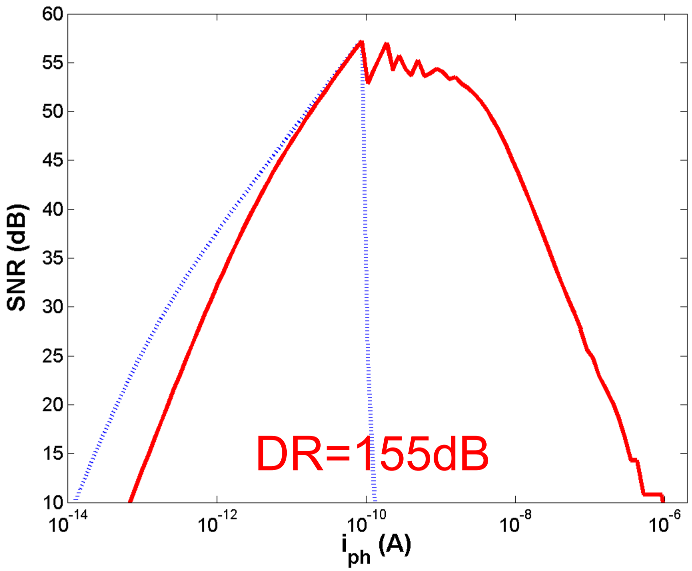
Multiple capture [Yang `99]

- ✓ High fidelity at both ends
- ✗ Cannot meet DR and speed requirements:
  - Per-pixel ADC speed/ resolution

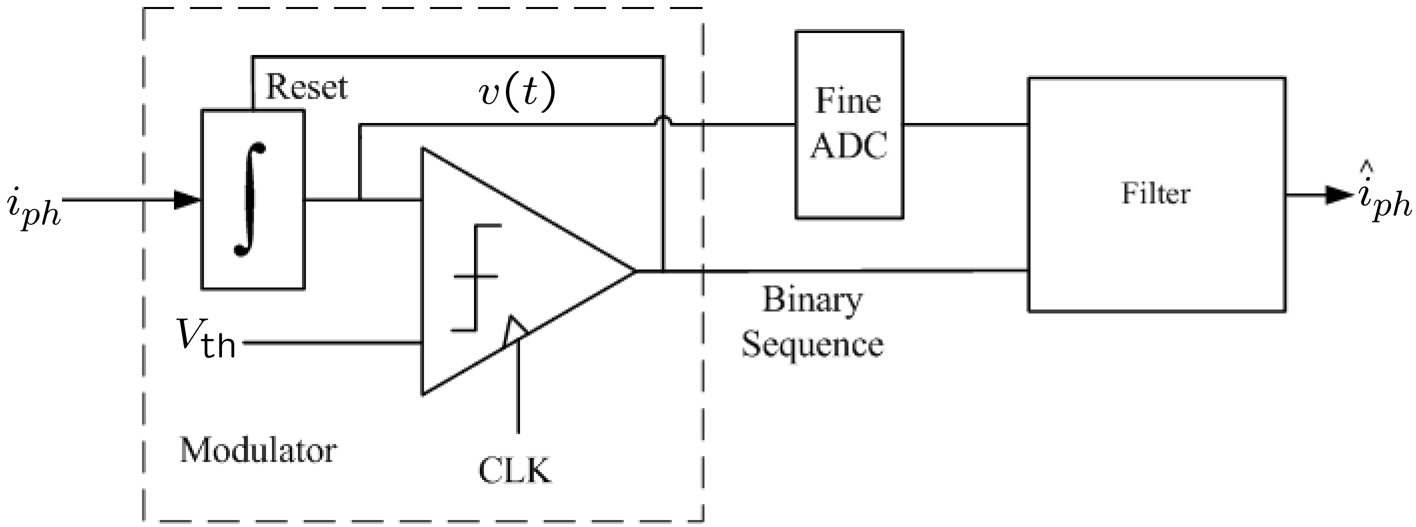


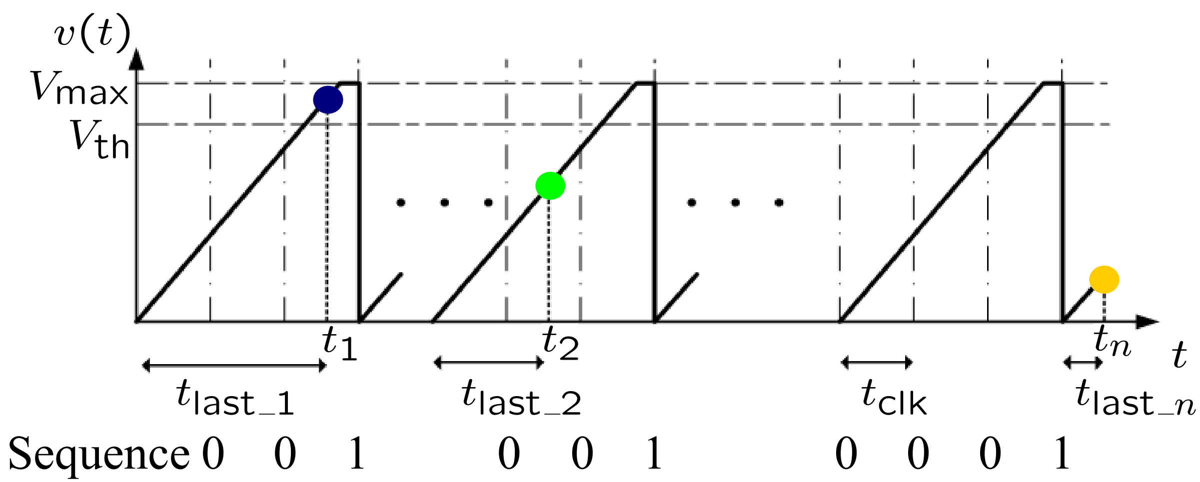
Synchronous self-reset [Rhee `03]

- ✓ Easily achieves DR and speed requirements
- ✓ Low power
- ✗ Poor SNR at both ends
  - Reset noise
  - Charge underestimation and offset accumulation

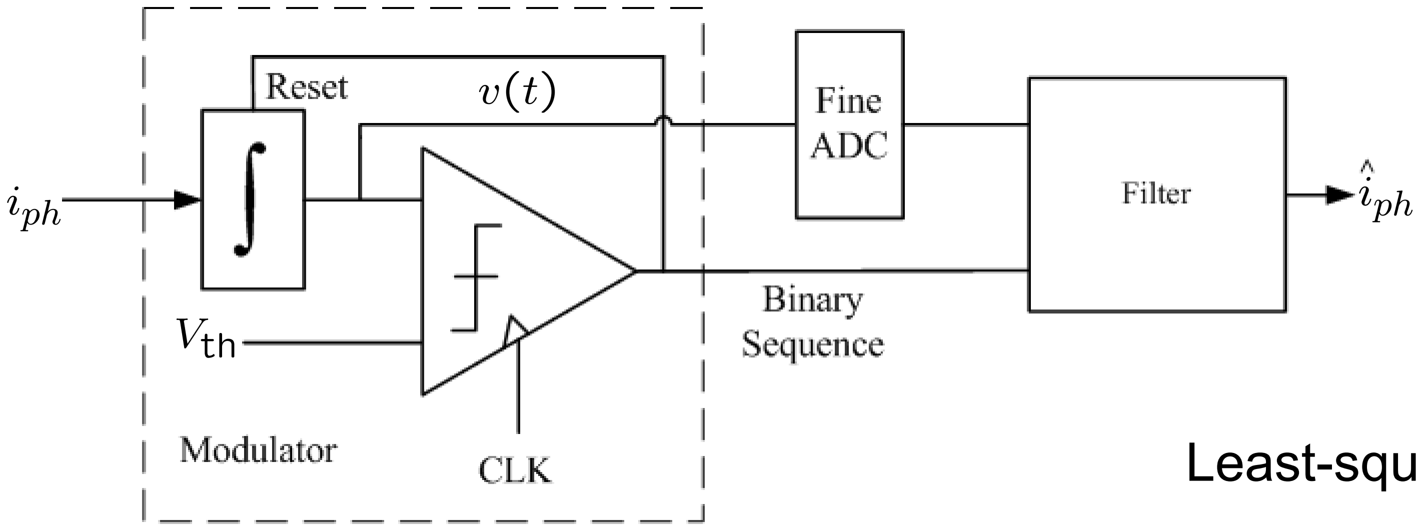


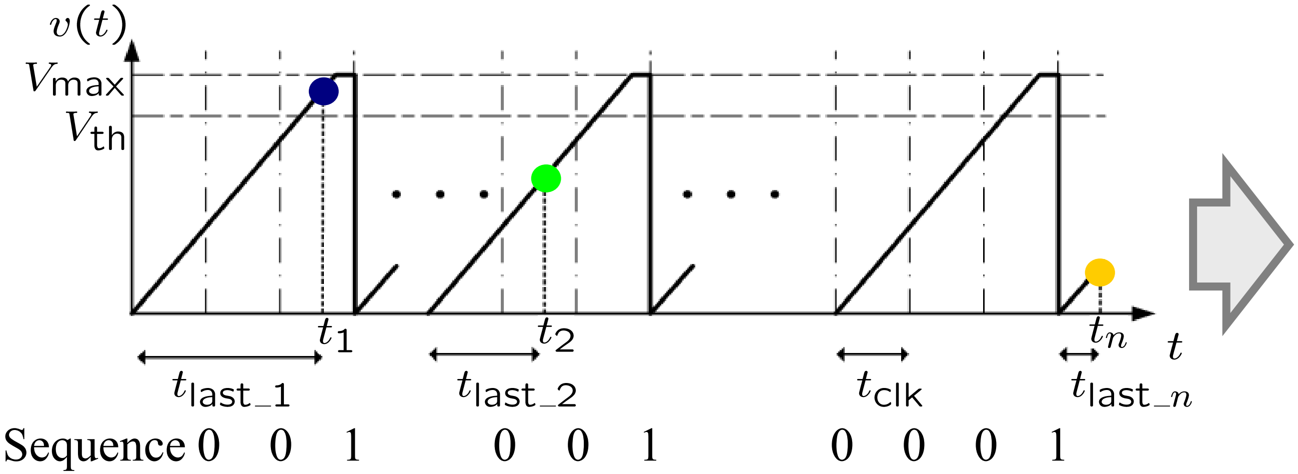
Folded Multiple Capture





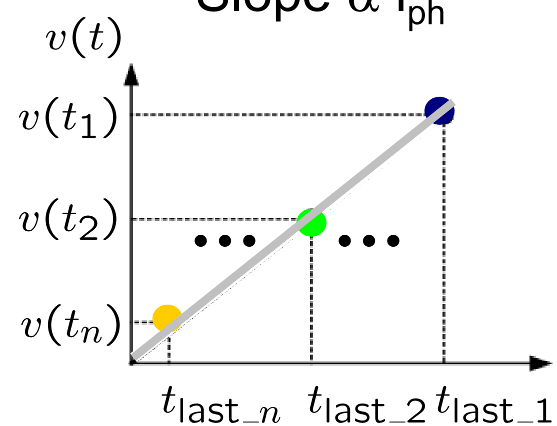
Folded Multiple Capture



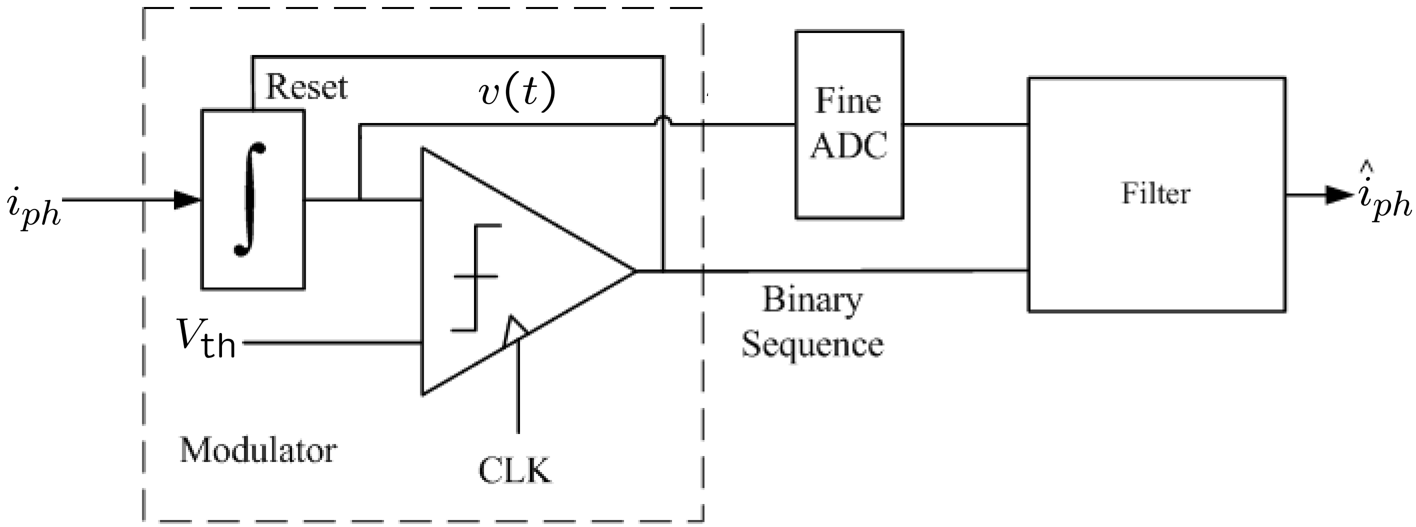


Least-squares fit

Slope α i_{ph}

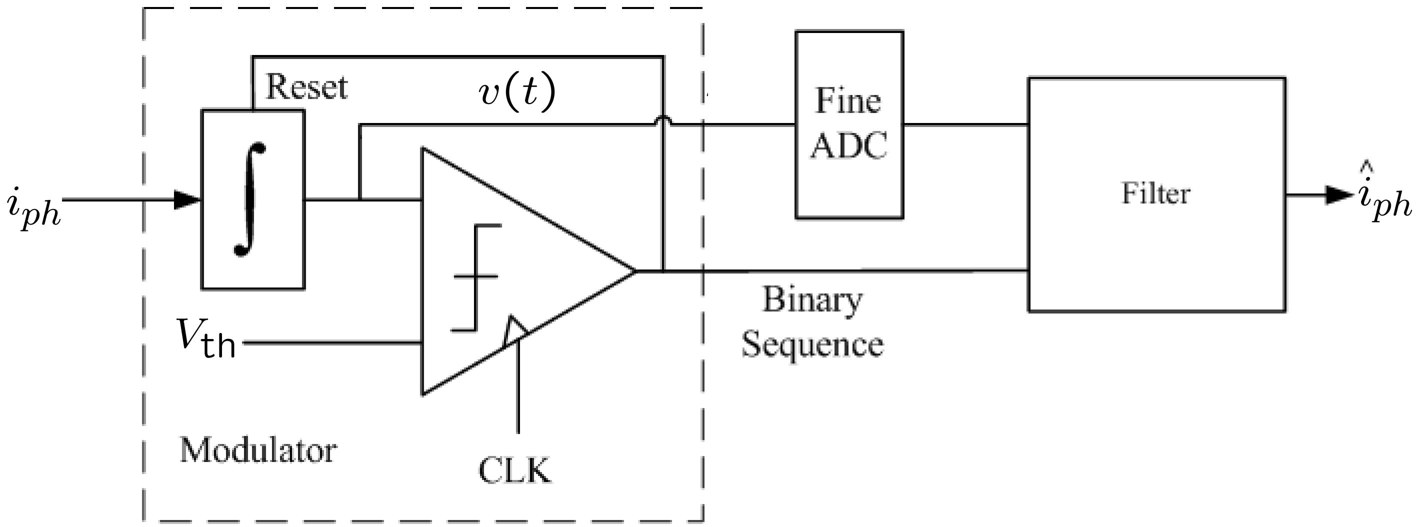


Folded Multiple Capture



- $i_{\text{min}} = q\sigma_{\text{Readout-eff}}/t_{\text{int}}$
  - Lower than reference sensor due to least-squares fit
- $i_{\text{max}} = 2qQ_{\text{max}}/t_{\text{clk}}$
  - Factor 2 due to 180^{o} phase shift between capture and reset clock

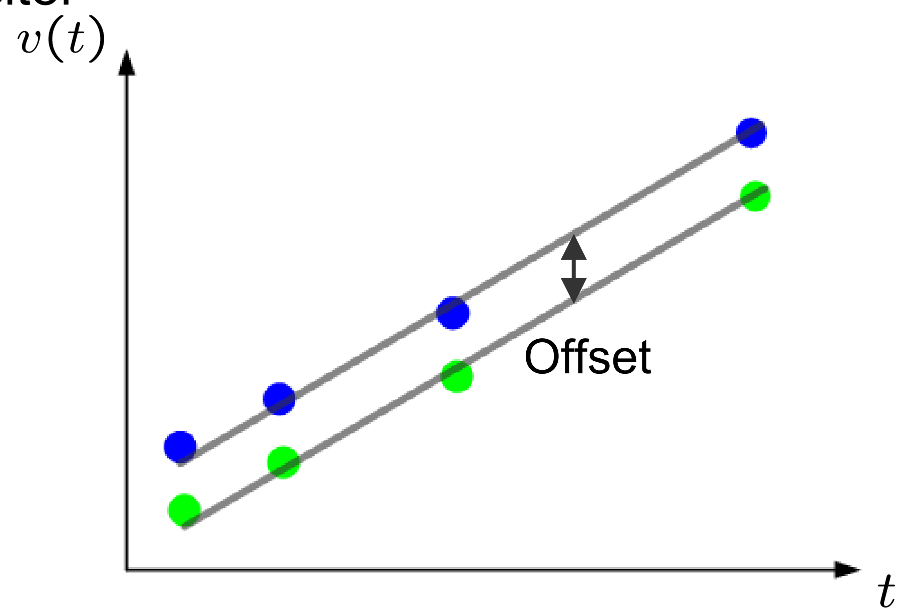
Folded Multiple Capture



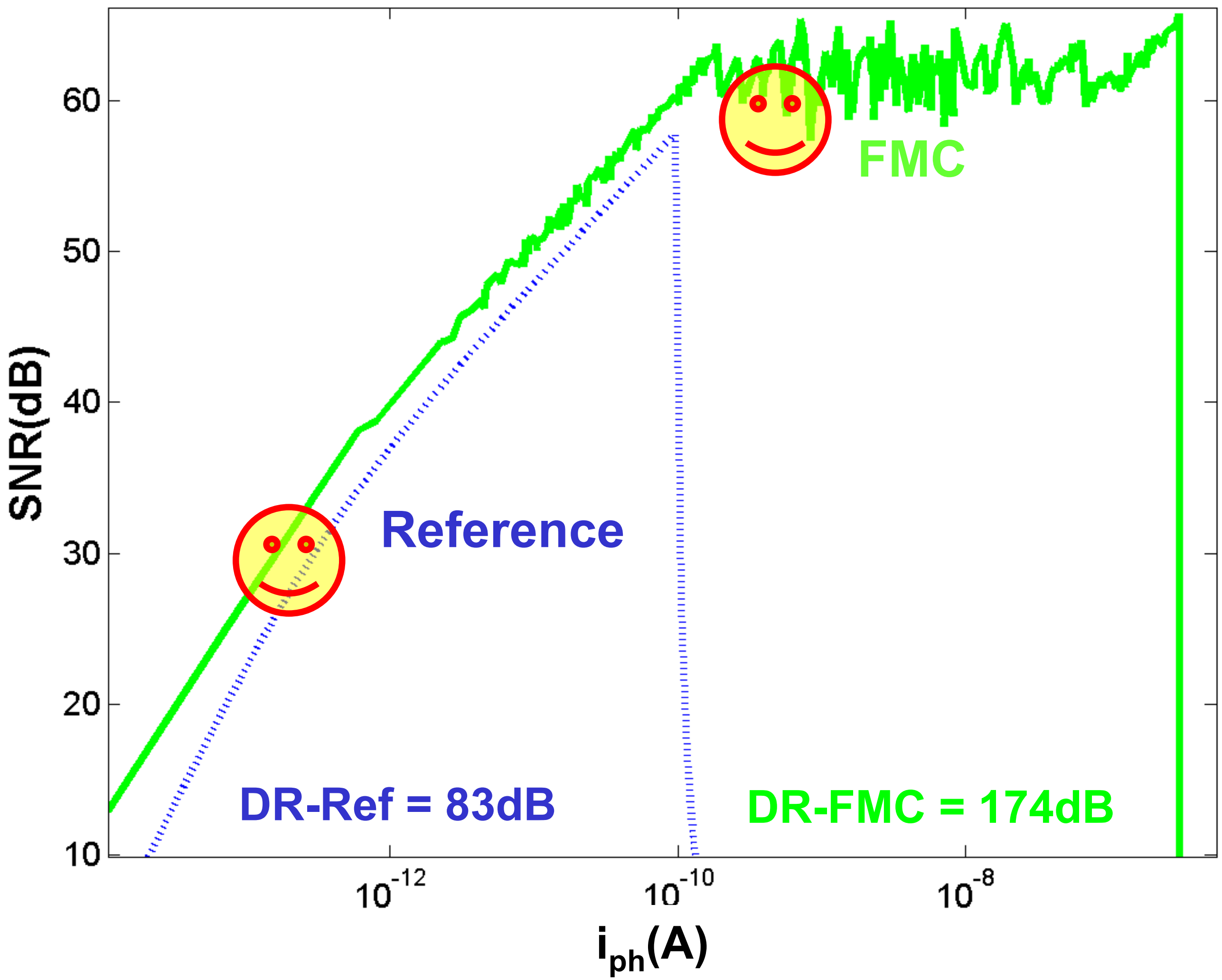
- Low end SNR limited by shot/read noise
  - ✓ Better than reference sensor due to least-squares fit
- High end SNR limited by well capacity
  - ✓ Also benefits from least-squares fit

FMC Robustness to Offset and Noise

- Least-squares estimation reduces
  - Offsets (also reset noise at low end)
  - Read and reset noise
  - 1/f noise [Fowler `91]
- This relaxes
  - ✓ Settling requirement of CTIA → relaxes its gain-bandwidth
  - ✓ Size of the sample-and-hold capacitor
  - ✓ Fine ADC resolution



SNR (4 Captures)



- Assumptions

$Q_{\text{max}} = 625,000e-$

$Q_{\text{th}} = 0.9Q_{\text{max}}$

$\sigma_{\text{Readout}} = 40e-$

$\sigma_{\text{Switch}} = 127e-$

$\sigma_{\text{Comparator}} = 1000e-$

$\sigma_{\text{Offset}} = 18000e-$

$t_{\text{int}} = 1m\text{sec}$

$t_{\text{clk}} = 1\mu\text{sec}$

$t_{\text{int}}/t_{\text{clk}} = 1000$

$t_1 = 148.5t_{\text{clk}}$

$t_2 = 335.5t_{\text{clk}}$

$t_3 = 502.5t_{\text{clk}}$

$t_4 = 969.5t_{\text{clk}}$

How Many Captures Are Needed?

- One capture is not enough to guarantee high SNR in the entire dynamic range
- Can we get away with few globally preset captures?
- Answer:
  - ✓ Yes. Can achieve high SNR over entire dynamic range with only 3-4 *global, scene independent* captures

Why One Capture is Not Enough?

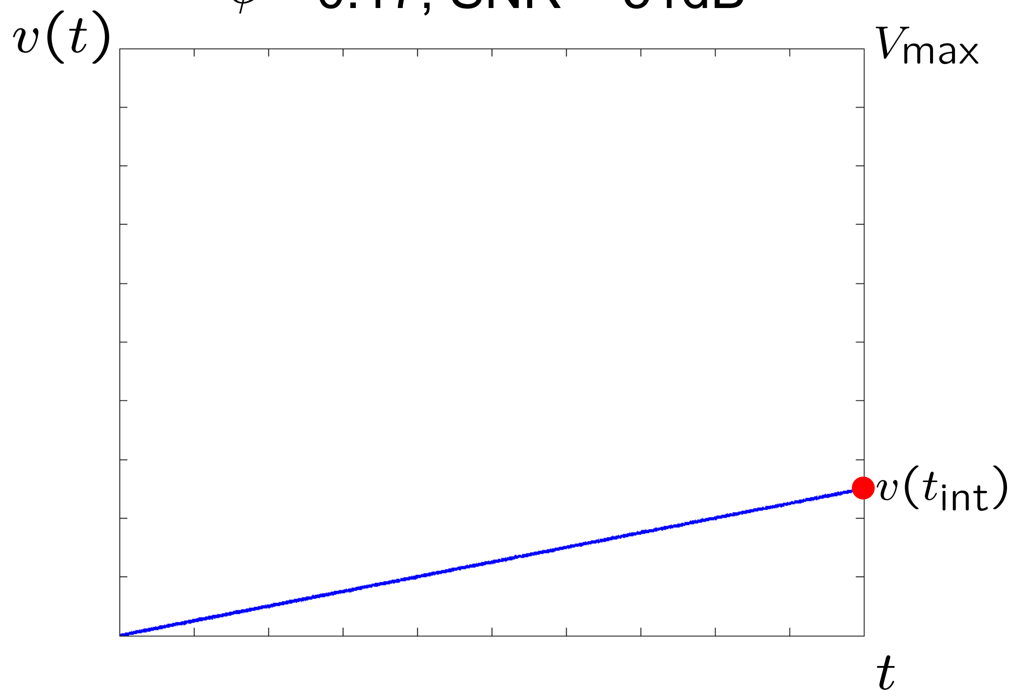
- Consider single capture at the end of integration time
- For $i_{ph} < qQ_{\text{max}}/t_{\text{int}}$
- Define

$$\phi(i_{ph}, t) = \frac{v(t_{\text{int}})}{V_{\text{max}}}$$

- Can show that

$$\text{SNR} \approx \phi(i_{ph}, t)Q_{\text{max}}$$

ϕ = 0.17, SNR = 51dB



max(SNR) = 58dB

Why One Capture is Not Enough?

- Consider single capture at the end of integration time
- For $i_{ph} > qQ_{\text{max}}/t_{\text{int}}$
- Define

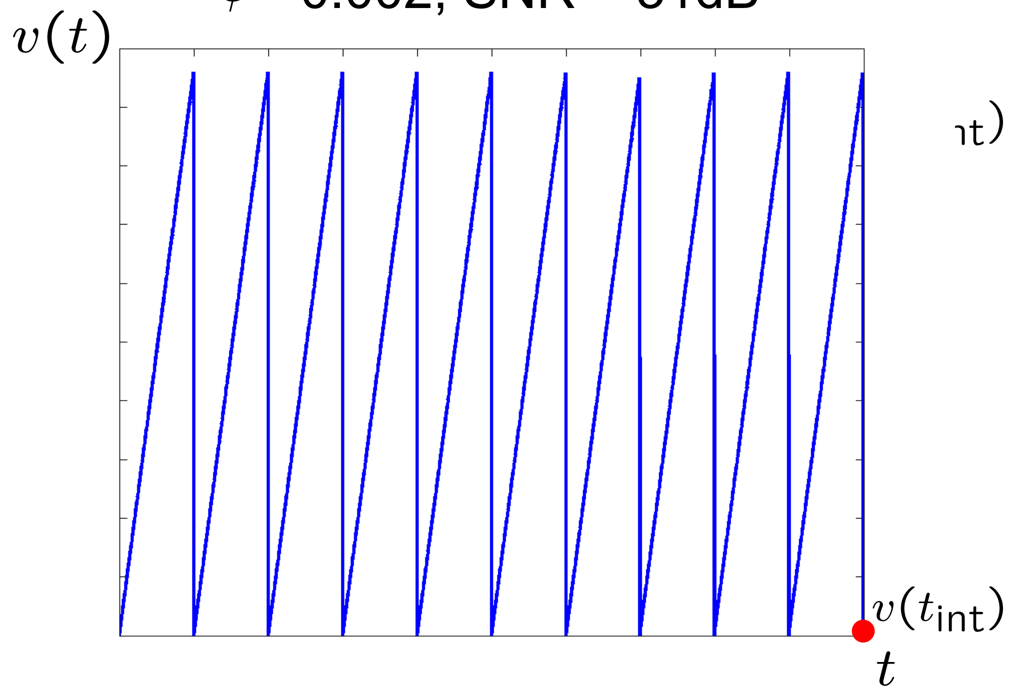
$$\phi(i_{ph}, t) = \begin{cases} \frac{v(t_{\text{int}})}{V_{\text{max}}}, & \text{if } \phi(i_{ph}, t) \le 1 \\ 0, & \text{otherwise} \end{cases}$$

- Can show that

$$\text{SNR} \approx \phi(i_{ph}, t) Q_{\text{max}}$$

✘ ϕ can be small

ϕ= 0.002, SNR = 31dB



max(SNR) = 58dB

Global Capture: Problem Formulation

Assuming n captures at $0 < t_1 < t_2 < t_n$ where $t_i \in \{(k_i + 1/2)t_{\mathrm{clk}}$, for $0 \leq k_i < t_{\mathrm{int}}/t_{\mathrm{clk}}\}$

Find smallest n and capture times $t_1, t_2, \ldots, t_n$ such that:

$\max_i(\phi(t_i)) > \alpha$ for all $i_{ph} > Q_{\mathrm{max}}/t_{\mathrm{int}}$ and $0 < \alpha < 1$

Global Capture Times

- Problem is in general NP-complete
- Developed a heuristic using greedy algorithm and found multiple solutions for different values of α

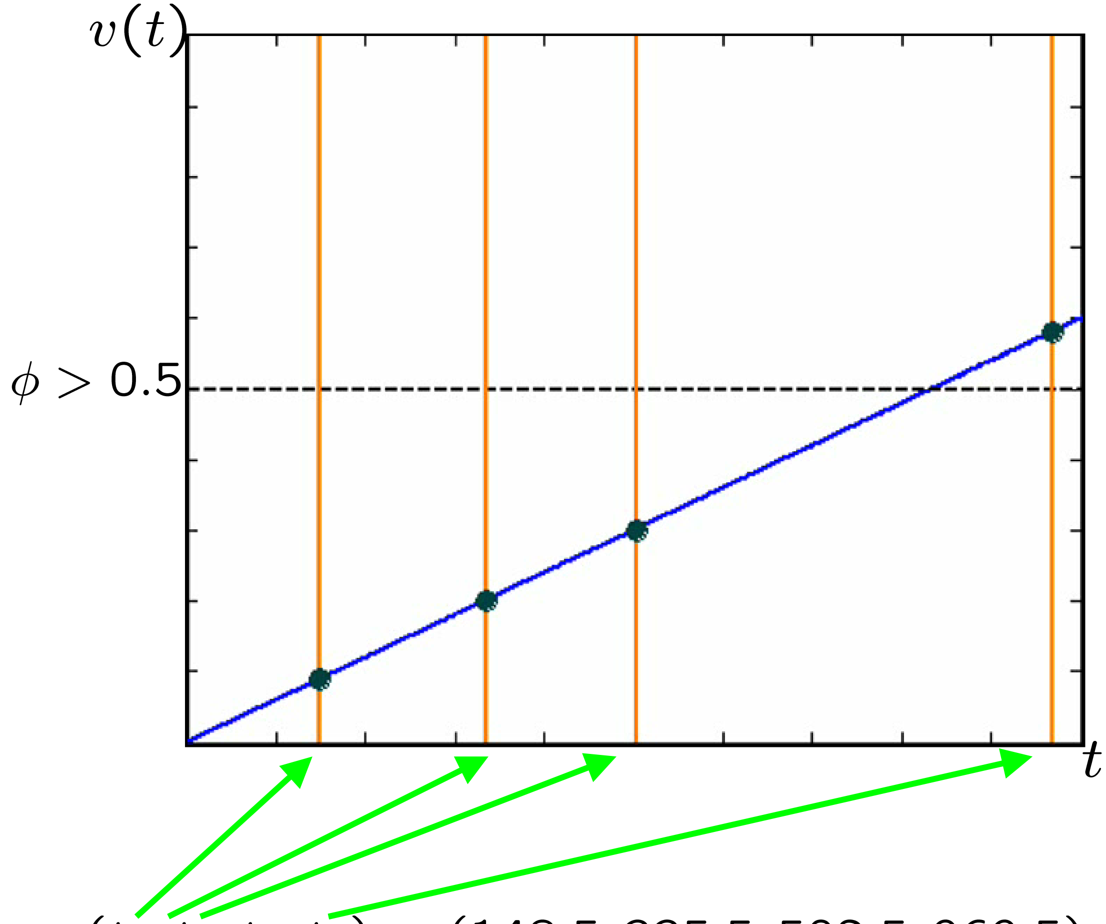
✓ Found that only few captures are needed

✓ For example: for $t_{int}/t_{clk} = 1000$

$\alpha = 0.5$	$(148.5, 335.5, 502.5, 969.5) \times t_{clk}$
$\alpha = 0.33$	$(143.5, 334.5, 818.5) \times t_{clk}$

Capture time solutions for two thresholds

Illustration



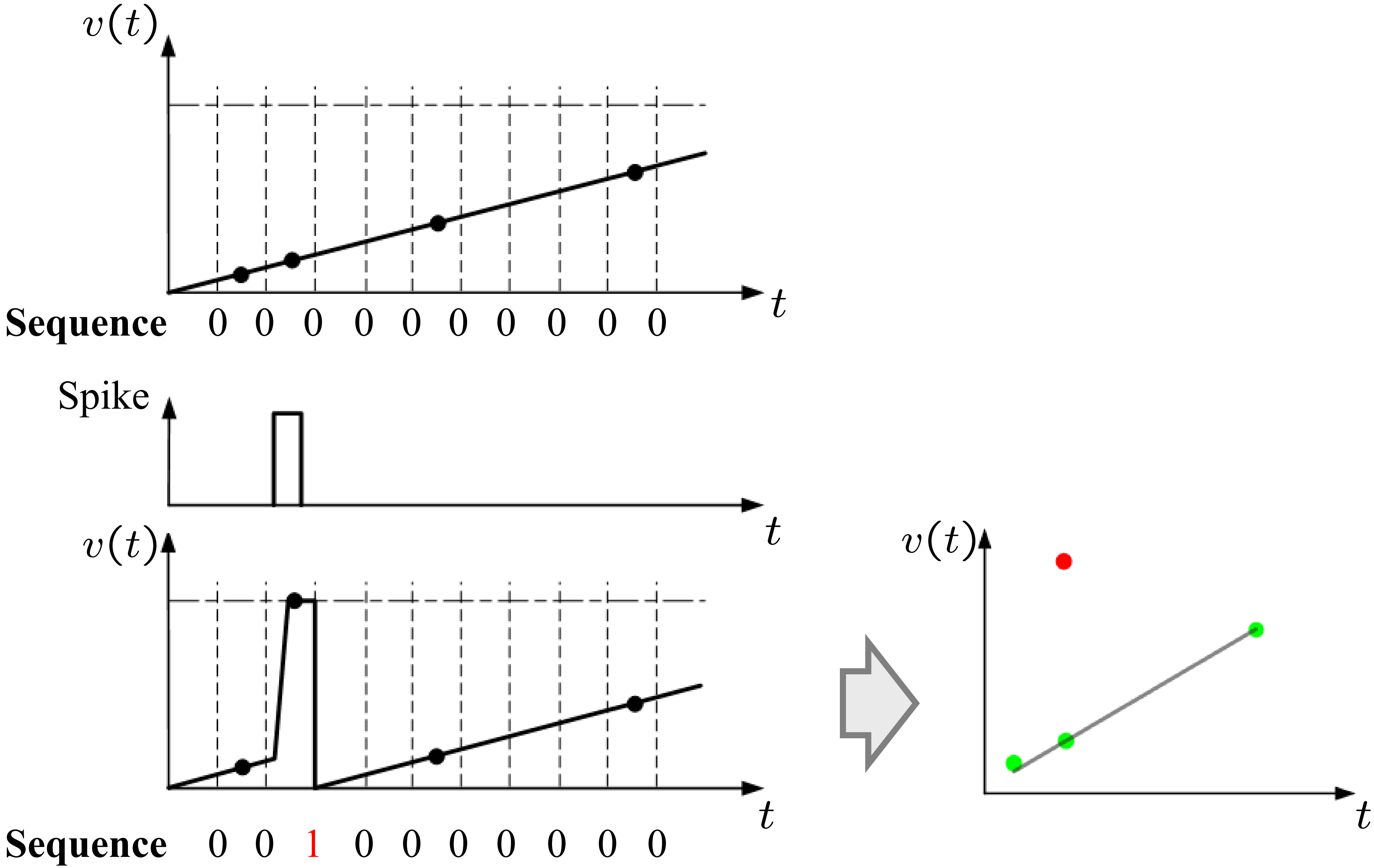
$$(t_1, t_2, t_3, t_4) = (148.5, 335.5, 502.5, 969.5) \times t_{\text{clk}}$$

Disturbance Problem

- Caused by sun reflection, laser jammer

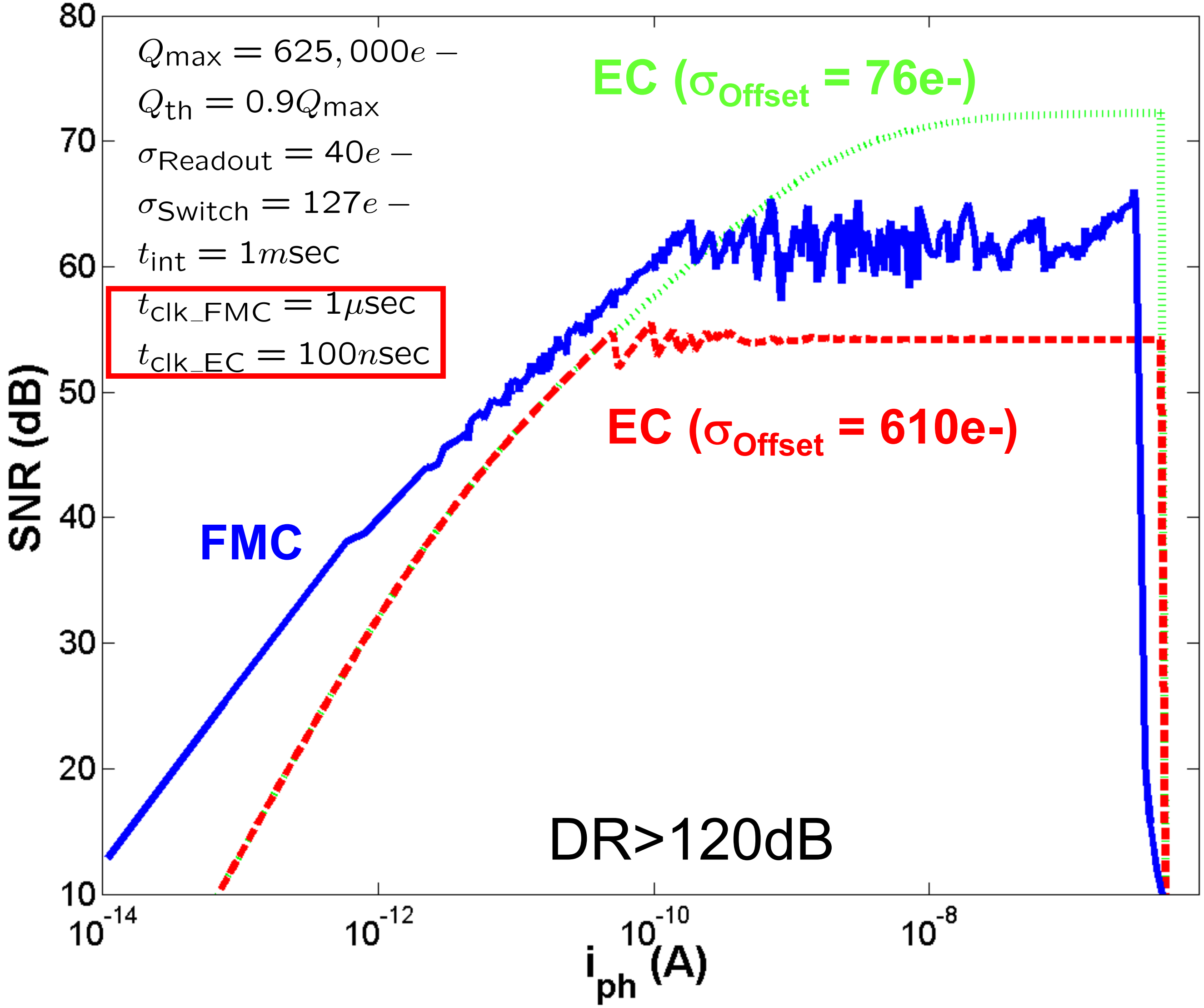
- Can be detected in conventional sensor using very *high* frame rate → high power and SNR degradation

Disturbance Tolerance in FMC



Disturbance Tolerance: Example

FMC versus Extended Counting



Power Consumption Comparison

- We show that FMC power consumption is significantly lower than that of extended counting
- Main reason:
  - Extended counting is a uniform 20-bit quantizer
  - FMC adapts integration time to signal level (AGC-like function) while maintaining high fidelity

Power Consumption for EC

- Power consumption for a 256 x 256 FPA employing extended counting at 1000 fps and 120dB DR
- View the whole ROIC as a data converter
- Assume FoM = Power/(2^{bits}x2BW) = 0.5pJ (aggressive) [Walden '99]
- Extended counting yields uniform quantization
  - 120dB = 20-bit of resolution
- Power estimate = 0.5p x 2^{20} x 1000 x 256^2

  = 34Watt

Power Comparison Assumptions

- CTIA is the dominant term in EC power
- For the same DR, extended counting requires at least 4x the clock rate of FMC

$$\frac{t_{\mathrm{clk}}(\mathrm{FMC})}{t_{\mathrm{clk}}(\mathrm{EC})} = \left(\frac{2Q_{\mathrm{max}}t_{\mathrm{int}}}{\sigma'_{\mathrm{Readout-eff}}}\right) \Big/ \left(\frac{Q_{\mathrm{max}}t_{\mathrm{int}}}{2\sigma_{\mathrm{Readout-eff}}}\right) \geq 4$$

- For same clock rate, CTIA settling time of FMC is relaxed compared to EC, can show that

$$\frac{\tau_{\mathrm{settle}}(\mathrm{FMC})}{\tau_{\mathrm{settle}}(\mathrm{EC})} \geq 2$$

- Conclusion: CTIA gain-bandwidth of EC is 8x higher than FMC

Power Consumption for FMC

- Assuming MOS square-law
  - CTIA power = $34/8^2$ < 1Watt
- Assuming fine ADC FoM of 0.5pJ
  - Fine ADC power < 1Watt
- Total FMC power consumption < 2Watt
- Compared to 34Watt for EC

Conclusion

- Described a new FPA ROIC scheme that:
  - Can achieve high dynamic range (>120dB) at high speed (>1000 frames/sec)
  - Maintains high fidelity in the entire dynamic range
  - Has low power consumption
  - Can detect and correct for subframe disturbances

- Well suited for vertical integration and achieves VISA requirements

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